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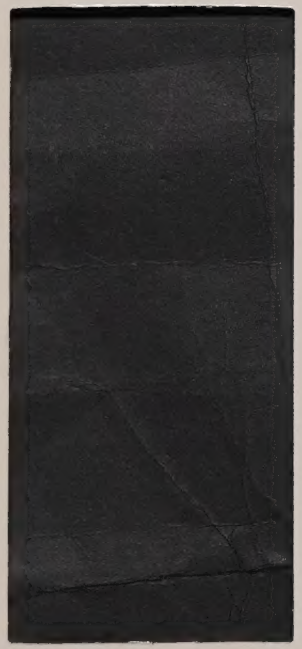

tau-tron
A UNIT OF
GENERAL SIGNAL

S5104 DS1/DS1C/DS2

DIGITAL TRANSMISSION TEST SET

OPERATION MANUAL

PART NO. 8200-0166

FORM 0309-0386D

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S5104 DS1/DS1C/DS2

DIGITAL TRANSMISSION TEST SET

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INTRODUCTION

This manual guides you in the use of the S5104 DS1/DS1C/DS2 Digital Transmission Test Set. The content, format, and style of the manual is new; it was written to give you a better understanding of the tests you perform with your S5104.

This manual is divided into three main parts: GETTING STARTED, TUTORIAL, and REFERENCE. GETTING STARTED describes the S5104 and explains unpacking and setup procedures. TUTORIAL is written to guide users in the use of the S5104 and to give them a general understanding of how to perform tests on digital facilities. REFERENCE contains detailed and comprehensive reference information.

We would appreciate your comments about any errors or omissions you discover in this manual. Utilizing the feedback card located in the back of this manual, please address all correspondence to:

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SECTION 1
S5104 DESCRIPTION

The S5104 Digital Transmission Test Set is a comprehensive instrument that allows you to test the performance of digital transmission systems operating at DS1, DS1C, and DS2 levels. It is ideal for testing digital radio, fiberoptic, satellite, and T-carrier systems including multiplexers, protection switches, and lines.

Many unique features and abilities are incorporated into this versatile and cost-effective test set. The unit can transmit framed and unframed data patterns and perform error measurements at all three transmission rates. The S5104 is capable of transmitting test patterns at one rate while performing measurements at another rate. Your S5104's ability to measure frame bit errors and bipolar violations (BPV's) allows you to monitor the performance of in-service systems. In addition to recognizing Alternate Mark Inversion (AMI) in DS1 signals, the S5104 can encode/decode Bipolar with 8-Zero Substitution (B8ZS) signals, making it an ideal instrument to develop and test DS1 equipment designed for 64-kb/s clear channel operation.

If your S5104 has the Jitter Injection/Measurement Option, it injects a programmable amount of jitter into signals with its own internal sinusoidal oscillator to simultaneously measure peak-to-peak jitter, +peak jitter, −peak jitter, jitter threshold seconds, and maximum jitter.

The S5104 provides jitter weighting filters compatible with the American National Standards Institute (ANSI) T1 Committee recommendations of December 1985.

NOTE: S5104's shipped prior to July 1986 may use different weighting filters. The relationships between the new and old jitter weighting filters are explained in PART 2, SECTION 5 of this manual.

You can perform simultaneous measurements of jitter, status event seconds, BPV's, and either bit errors or frame bit errors with your S5104. Furthermore, a THRU mode permits you to add jitter, BPV's, or bit errors to in-service facilities or user-generated signals for performance testing of protection switches, channel banks, and other equipment under controlled conditions.

SECTION 2
UNPACKING INSTRUCTIONS

After removing your S5104 from the shipping container, remove the front-panel cover and open the black plastic bag attached to the inside of the cover. You should find a 10–foot (3–meter) AC power cord and a spare fuse inside this bag.

TURNING ON THE POWER

Plug the 3-wire AC power cord into the 115–Vac or 230–Vac power connector (depending on the power version you ordered) on the rear panel of your S5104. Then plug the power cord into a properly grounded outlet. Press the POWER pushbutton on the front panel; it lights to show the S5104 is turned on.

When the S5104 is powered up, all the front-panel indicators light for a few seconds. The following default indicators remain lit:

TRANSMITTER OUT

- DSX1
- PRBS
- UNFRAME

ERROR INJECT

- BIT
- ERR FREE
- MODE

MEASUREMENT TIME

- UNTIMED
- IN PROC

MEASUREMENTS

- BIT

RECEIVER INPUT

- UNFRAME
- PRBS
- DSX1

INPUT

- DS1/1C/2 (left)

If the above indicators are not lit, refer to SECTION 10, SERVICE AND MAINTENANCE, in the reference part of this manual.

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INTRODUCTION

This part of the manual contains instructions on how to use Tau-tron's Model S5104 DS1/DS1C/DS2 Digital Transmission Test Set. You will learn the measurement capabilities of your S5104 and how to use your set to monitor and test digital performance.

This part also explains how to understand and use the Jitter Measurement and Injection option.

SECTION 1
AN INTRODUCTION TO DIGITAL PERFORMANCE TESTING

1.1 WHAT IS DIGITAL PERFORMANCE TESTING?

The most accurate way to measure the quality of a digital path, such as a T1 spanline, is through a bit-by-bit error check. This test requires transmitting a known data bit pattern over the digital line and then comparing the received bit pattern to the expected bit pattern. Any differences between the received and the expected bit pattern are considered bit errors. This test offers the highest level of error detection; theoretically 100%.

Bit-error tests can only be performed on out-of-service digital paths because the bit pattern of live traffic is unknown. Often a line cannot be taken out of service for testing. Therefore, a different test is required to test in-service digital paths.

How then do we check the quality of an in-service digital path? Two other characteristics of a live traffic signal can be monitored to effectively check for the quality of a digital path: Bipolar Violations (BPV's) and Frame Bits (these will be explained shortly). These characteristics can be monitored and measured without interfering with live traffic, although the results do not provide the resolution and accuracy of bit-error tests.

The S5104 tests the quality of digital paths that transmit data at DS1, DS1C, and DS2 transmission rates. These rates are three of the standard rates of the North American digital hierarchy. Bit errors, BPV's, and frame bit errors can be measured by your S5104 at any of these rates.

In summary, digital performance testing is the monitoring and measuring of bit errors, BPV's, or frame bit errors over a period of time at DS1, DS1C, and DS2 transmission rates. We will now explain these measurements in more detail.

1.2 WHAT ARE BIT ERRORS?

All digital transmission systems are based on the binary system in which information is made up of 1's (ones) and 0's (zeros). Each of these 1's and 0's is called a bit, short for binary digit. Bits are transmitted in the digital signal as a stream of "pulses" (also called marks) and "spaces" representing binary 1's and 0's respectively.

Bits are initially generated and eventually decoded (received) as unipolar data; these pulses can vary in only one polarity. In unipolar format, binary data is encoded into two logic levels (e.g., high = 1, low = 0). Unipolar logic levels vary from system to system. Figure 1 illustrates an example of a unipolar bit signal.

A bit is considered errored if it is not received at the same logic level as originally transmitted. Bit errors are detected and measured by comparing a known sequence of transmitted bits to the received bits. Any bits that do not match are called bit errors.

Several different bit patterns can be transmitted by the S5104 for performance testing. If the S5104 detects 12 or more bit errors out of 40 bits when comparing these bit patterns, the signal is considered to be out of synchronization. An indicator lights to inform you of this condition.

1.3 WHAT ARE BIPOLAR VIOLATIONS?

DS1, DS1C, and DS2 signals are transmitted in a bipolar format that comprises positive and negative polarity pulses. One type of bipolar *line code* is called AMI (Alternate Mark Inversion). In an AMI signal, pulses *always* alternate in polarity. The positive and negative pulses represent binary 1's, while the absence of a pulse represents a binary 0. Figure 2 illustrates a typical bipolar binary signal.

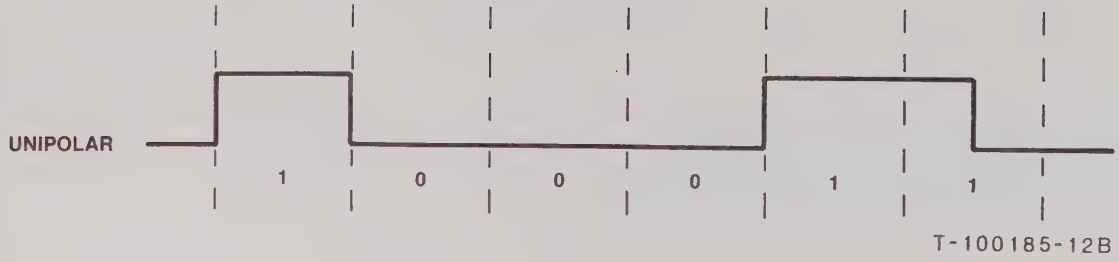

Fig. 1 – Unipolar Bit Sequence

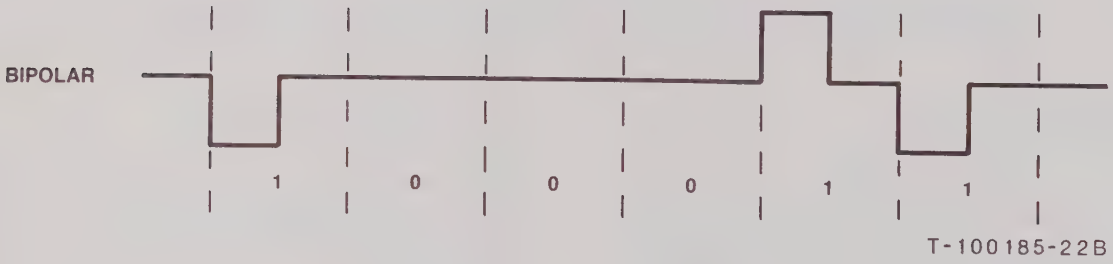

Fig. 2 – Bipolar Signal

The most important point to remember about AMI signals is that the positive and negative pulses always alternate. If two positive or negative pulses occur (whether separated by 0's or not), the bipolar code has been violated. This error condition is called a Bipolar Violation. Figure 3 shows an example of a bipolar violation.

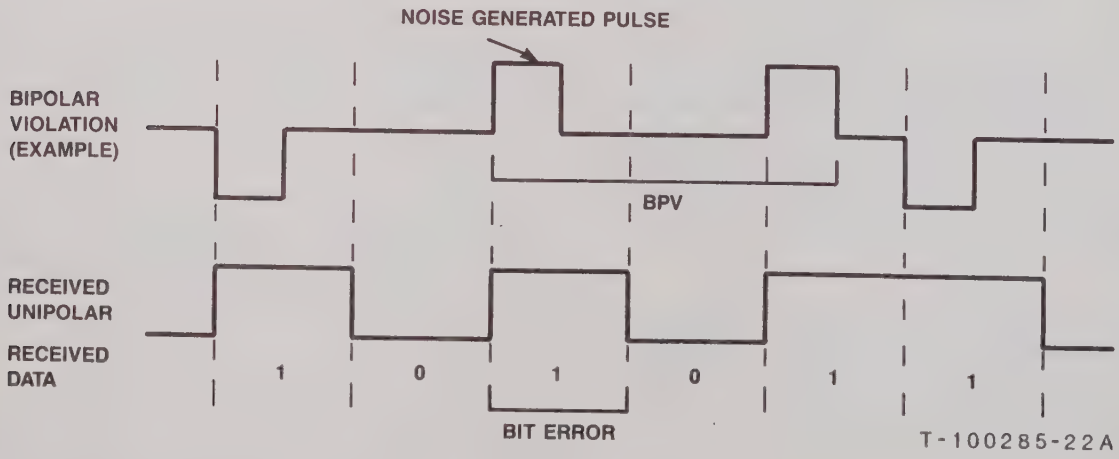

Fig. 3 – Bipolar Violation

In addition to AMI, some DS1 systems use a modified bipolar line code called Bipolar with 8-Zero Substitution (B8ZS). As in the AMI format, the polarity of 1's *normally* alternates in this format, but a special code word, containing intentional BPV's (for identification), is substituted when eight 0's occur in a row in the original signal. This prevents a loss of energy in DS1 signals compatible with 64-kb/s *Clear Channel* Capability (64 CCC), which would cause a loss of timing synchronization. The S5104 is capable of recognizing B8ZS code words in B8ZS formatted signals and detecting BPV's that result from transmission errors or either AMI or B8ZS formatted signals.

1.4 WHAT ARE FRAME BIT ERRORS?

A DS1 signal is composed of multiple "information" channels (normally 24 DS0, 64-kb/s channels) that are transmitted sequentially. Information bits are grouped into *FRAMES*. A framing bit is inserted at the beginning of each frame to permit correct decoding and demultiplexing of the signal at the Receiver. Figure 4 shows how frame bits are inserted into a DS1 signal.

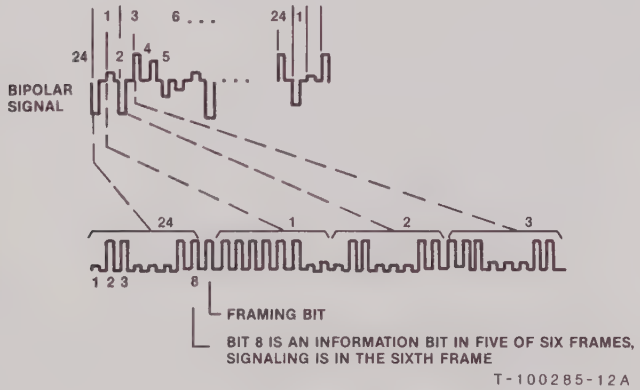
1 3 6 . . . 24 1
24 2 4 5
BIPOLAR SIGNAL
24 1 2 3
1 2 3 8
FRAMING BIT
BIT 8 IS AN INFORMATION BIT IN FIVE OF SIX FRAMES, SIGNALING IS IN THE SIXTH FRAME
T-100285-12A

Fig. 4 – Frame Bit Sequence

A known, fixed framing bit pattern allows the Receiver to identify the beginning of each frame. Each frame contains 193 bits with the frame bit as the last bit. The DS1 rate transmits 8000 frames per second (1.544 megabits per second), consisting of 8000 frame bits plus 1.536 million information bits.

Framing bits are also used in DS1C and DS2 signals. Each DS1C signal consists of 3.152 million bits transmitted each second. Approximately 3.092 million are information bits and 60 thousand are control bits. One-third of the control bits are F-bits (frame bits). Each DS2 signal consists of 6.312 million bits transmitted each second. Approximately 6.183 million are information bits and 129 thousand are control bits. One-third of the control bits are F-bits.

A frame bit error occurs when the received frame bit pattern does not match the expected pattern. Excessive frame bit errors can cause an out-of-frame condition that results in a loss of synchronization. This generally happens only during periods of very high error rates. At the DS1 rate, the S5104 detects a frame loss when three frame bits out of six are in error. For DS1C and DS2 rates, the S5104 detects a frame loss when three or more frame bits in one master frame are in error.

1.5 WHAT ARE DS1, DS1C, AND DS2 BIT RATES?

A digital hierarchy exists defining the relation of digital transmission systems that operate at different bit rates. This hierarchy segregates the various signals into building blocks which may be interconnected to make up transmission systems. All transmitted signals enter and leave the digital hierarchy by means of some type of signal conversion terminal. Figure 5 shows the part of the digital hierarchy that involves DS1, DS1C, and DS2 bit rates. The S5104 tests performance at all three bit rates.

The DS1 bit rate was initially used by the Bell System for short-haul digital transmission over T1 lines (paired cable systems). The DS1 signal is a 1.544-Mb/s pulse stream that is transmitted in a bipolar format. This signal is made up of 24 DS0 channels (other channelization schemes exist). Each channel is transmitted at a bit rate of 64 kb/s (the DS0 bit rate). The 24 channels are multiplexed, along with framing bits to segregate the channels, to form a DS1 signal.

Transmission bit rates above DS1 are formed by multiplexing two or more DS1 signals. For example, the DS1C bit rate is just over twice that for DS1 signals and (normally) provides 48 channels for transmission. The bit rate of the DS1C signal is 3.125 Mb/s.

In performance testing, framed DS1C or DS2 bit patterns consist of two or four DS1 pseudorandom bit sequences (with 14-zero constraint) mixed together with proper frame bits. An unframed DS1C or DS2 bit pattern consists of either a 2^{20} -1 PRBS (with 19-zero constraint) or a fixed bit pattern.

A DS2 signal is composed of four multiplexed DS1 signals with a transmission rate of 6.312 Mb/s. The DS2 signal uses a modified bipolar format called Bipolar with 6-Zero Substitution (B6ZS). As in the DS1 signal, 1's alternate in polarity, but a special code word is substituted when six 0's occur in a row (using a scheme similar to the DS1 B8ZS line format). This ensures that loss of energy in the signal does not cause a loss of synchronization.

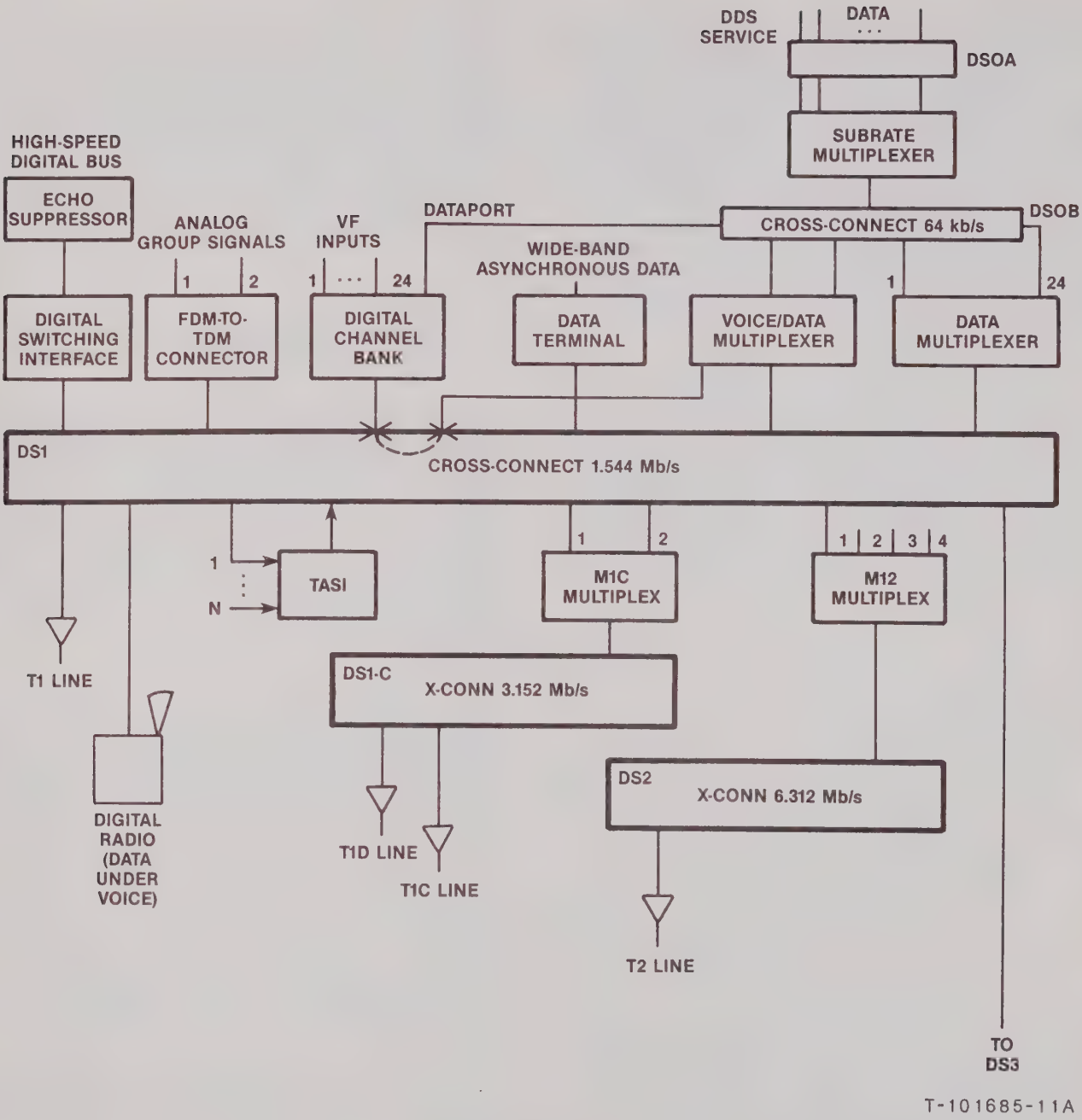

Fig. 5 – DS1, DS1C, and DS2 Digital Hierarchy

SECTION 2

WHAT DOES THE S5104 MEASURE?

2.1 S5104 MEASUREMENT CAPABILITIES

The S5104 measures bit errors, frame bit errors, BPV's, and status-event seconds. If your S5104 has the jitter measurement option, it also measures jitter. Jitter measurement is explained at the end of this section.

The S5104 calculates several different measurements for each test. You can read the results of these measurements from the front-panel display or from the printed Summary Report. You can perform appropriate measurements on unframed, framed, and live signals. The following measurements are available:

- Total Errors – Total number of errors that occur in the elapsed test time.
- Average Error Rate – Average error rate over time of test.
- Total Errored Seconds – Total number of seconds in which an error occurred.
- Threshold Errored Seconds – Total number of seconds in which the error rate exceeds 1×1^{-5}, 1×10^{-4}, and 1×10^{-3} (E–5, E–4, and E–3). Not measured for frame errors.
- Dribbling Errors – Total accumulated errors that occur when the error rate is less than 1×10^{-6} in an errored second. Not measured for frame errors.

"Errors" is the generic term for bit errors, BPV's, or frame bit errors.

2.2 STATUS EVENTS

The S5104 detects and monitors six Status Events. Front-panel STATUS indicators alert you to the occurrence of these status events. These indicators light continuously while the event occurs or flash to show an event has occurred during the current test. In addition, Summary report printouts give a STATUS SECOND SUMMARY showing the number of seconds an event occurred during the test.

The six status events are:

- Signal Loss – A loss of signal is indicated if no bipolar pulses are detected for 25 microseconds ±10%. If at least one bipolar pulse is detected during a 25-microsecond interval, the S5104 recognizes a signal.
- Frame Loss – For DS1 signals, framing is considered lost when three out of six frame bits are in error. When 10 consecutive error-free frame bits are detected after a loss of frame, framing is considered regained. For DS1C and DS2 signals, framing is considered lost when three or more frame bits are in error in one master frame. When eight consecutive error-free frame bits are detected after a loss of frame, framing is considered regained.
- Sync Loss – For PRBS, indicates a loss of pattern sync if 12 bit errors are detected in a 40-bit data block. A signal is considered to have regained sync when 40 consecutive bits are transmitted without errors.

  For FIXED WORD:
  2 out of 40 = sync loss
  40 bits without errors = regained sync
- Detect Zeros – Indicated when an excessive number of consecutive 0's are detected in the bipolar signal. The number of consecutive 0's required to establish a DETECT ZEROS status is:

• DS1 AMI	16 or more
• DS1 B8ZS	8 or more
• DS1C	34 or more
• DS2	6 or more

- Detect All 1's – Indicated when an excessive number of consecutive 1's are detected in the bipolar signal. The number of consecutive 1's required to establish a DETECT ALL 1's status is:

• DS1 framed/unframed	1,000 ± 200
• DS1C framed	1,000 ± 200
• DS1C unframed	2,000 ± 400
• DS2 framed	1,000 ± 200
• DS2 unframed	4,000 ± 800

- Detect X-Bit – The S5104 detects X-Bits as logic 0. These are slow-speed signaling bits definable by the user. Status ON, X-Bit = 0. Status OFF, X-Bit = 1.

2.3 SYNCHRONOUS VS. ASYNCHRONOUS ERRORED-SECOND MEASUREMENTS

The errored second is one of the most important parameters used to express digital-facility error performance. Errored seconds are defined as one-second intervals in which there are one or more errors.

There are two methods for measuring errored seconds: asynchronous and synchronous. The asynchronous method of errored-second measurement utilizes a real-time clock, which is *not* synchronized to bit errors, to define 1-second periods. Synchronous errored-second measurement utilizes a 1-second interval that starts at the detection of the first error of an error event, which may be either a single (isolated) error, a group of errors, or an error burst (usually an error rate greater than 10^{-3}). Synchronous errored seconds are considered to be synchronized with error events.

Asynchronous and synchronous errored-second measurements may yield different results. Synchronous measurements yield the lowest possible number of errored seconds for a particular error distribution. The most important quality of synchronous errored-second measurements is that multiple instruments measuring the same transmission give identical results. The differences between asynchronous and synchronous measurements are illustrated in Figure 6.

Your S5104 performs synchronous errored-second measurements. However, if you have a need for asynchronous measurements, you may change to asynchronous by switching a DIP switch as explained in PART 3, SECTION 8.

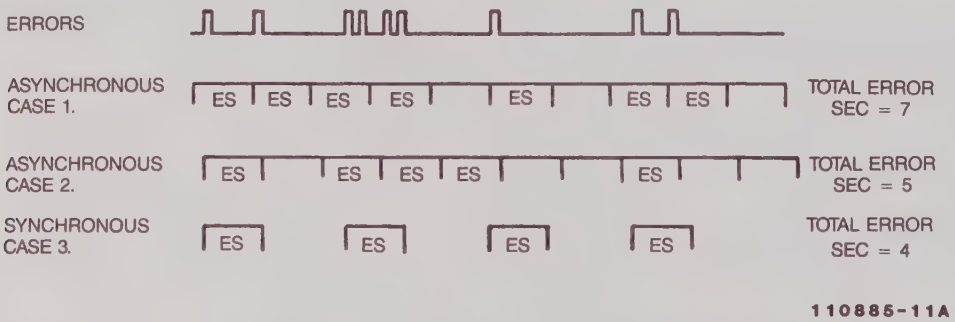

Fig. 6 – Synchronous vs. Asynchronous Errored-Second Measurements

SECTION 3

HOW TO DO PERFORMANCE TESTING ON A TEST-SET GENERATED SIGNAL

You can use your S5104 to test the performance of digital facilities by using loop-back and end-to-end techniques to perform logical bit-by-bit error checking. The following discussions present you with explanations and examples of tests using timed modes and error injection.

3.1 USING THE PSEUDORANDOM BIT SEQUENCE FOR PERFORMANCE TESTING

Your S5104 is capable of transmitting and recognizing a long bit pattern called a pseudorandom bit sequence (PRBS). The PRBS consists of 20^{20} –1 (1,048,575) bits; a pattern long enough to simulate the characteristics of live traffic. The DS1 PRBS is limited to 14 consecutive 0's. DS1C and DS2 PRBS's are limited to 19 consecutive 0's.

The PRBS can be used at any of the DS levels in either a framed or unframed format. In a framed PRBS, there is no synchronization between the PRBS and the frame bits; frame bits are inserted independent of the PRBS. Frame bits are "gapped" into the PRBS and do not overwrite the PRBS data bits.

The PRBS is used as a foundation for performing various tests. For example, two S5104's can be set up at each end of a line to be tested. One S5104 is set to transmit a PRBS at the desired DS level and frame format. The other S5104 is set to receive the signal. The receiving S5104 synchronizes with the transmitted PRBS and compares the bits actually received with the bits expected in the PRBS. Received bits that do not equal bits expected in the PRBS are recognized as bit errors by the S5104. Your S5104 automatically counts bit errors during a test.

Bit errors can be deliberately injected into the PRBS using the S5104 transmitter. The primary use for injecting bit errors is "signal tagging." When testing a digital path, bit errors can be injected into a test signal to confirm that the signal being received is the same as the signal being generated. At the end of a test, your S5104 automatically performs several calculations based on the detected bit errors. In addition to the total number of bit errors, you can immediately review the average error rate, the number of errored seconds, the number of dribbling errors, the percentage of error-free seconds, and the current error rate.

3.2 USING SHORT FIXED PATTERNS FOR PERFORMANCE TESTING

Short, fixed-bit patterns can be transmitted and recognized by your S5104. These fixed patterns are useful for testing the tolerance of a line repeater or network element (channel bank, DACS, etc.) to low-density patterns and excessive zeros.

In general, T1-line repeaters were designed to accept a maximum of 15 consecutive zeros and an average minimum pulse density of 12.5%, or one 1-bit out of every eight bits. Signals which use a bipolar code format (AMI) are considered to have excessive zeros if greater than 15 consecutive zeros occur. Signals using a B8ZS code format are considered to have excessive zeros if greater than seven consecutive zeros occur. In B8ZS-formatted signals, a zero substitution code replaces each string of consecutive zeros.

Before performing tests with short fixed patterns, set the rear-panel PROGRAMMABLE FIXED WORD DIP switches to the desired bit pattern. Next, set the DS1 OUTPUT toggle switch on the rear panel to either BIPOLAR or B8ZS. If you wish to perform tests using eight or more zeros, you *must* set the toggle switch to BIPOLAR.

3.3 USING THE ALL ONES BIT PATTERN FOR PERFORMANCE TESTING

A data pattern consisting of all ones is the easiest pattern to regenerate on digital lines. In some cases, a faulty repeater will regenerate an all ones pattern but not a pseudorandom pattern. Therefore, the all ones pattern can be used to test the severity of the problem.

The DS1 Alarm Indication Signal (AIS) is an unframed all ones bit pattern. Channel banks must respond to an AIS. Your S5104's capability to transmit an all ones bit pattern allows you to test the response of digital terminals to the AIS pattern.

SECTION 4

HOW TO DO PERFORMANCE TESTING ON IN-SERVICE FACILITIES

You can use your S5104 to check the quality of in-service facilities. Because the bit pattern of an in-service facility is unknown, you cannot use bit-error measurements. However, BPV's and frame bit errors can be monitored with your S5104. The following discussion presents you with explanations and examples of how to monitor BPV's and frame bit errors for in-service facilities.

4.1 MONITORING BIPOLAR VIOLATIONS

In a bipolar code format, 1-bits (pulses) must alternate in polarity regardless of the bit pattern transmitted. Whenever a bipolar violation is detected, an error has occurred in one of the bits between and including the pulses indicating the violation. This characteristic of BPV's gives you the opportunity to monitor the quality of the line without any knowledge of the nature of the traffic being transmitted.

To monitor BPV's in an in-service facility, set your S5104 Receiver to: LIVE FRAME, BPV's at the desired DS level. Your S5104 counts the total number of BPV's and calculates the number of errored seconds, the average error rate, the number of dribbling errors, and the percentage of error-free seconds.

You can inject BPV's into an in-service facility with your S5104 Transmitter when you set the TRANSMITTER OUT PATTERN to THRU. The signal is input to the Receiver as described above. With the Transmitter set to THRU, BPV's can be injected either singly or at a programmed error rate. Injecting BPV's into the signal allows you to perform tests on devices that detect BPV's, such as automatic protection switches.

4.2 MONITORING FRAME BIT ERRORS

In some situations error performance cannot be completely determined by monitoring BPV's. For example, multiplexes correct all BPV's through a function called Violation Monitor and Removal (VMR). Therefore, in general, BPV monitoring cannot indicate end-to-end performance on any path containing a multiplex. This situation is becoming more common as more high-speed fiberoptic and digital radio systems are introduced in the network.

Frame bit errors are not corrected by multiplexes and can be monitored at any point in the digital path. However, framing bits in DS1 signals only occur once every 193 bits in the data stream. This means that bit errors can be detected, at best, with a resolution of 1 in 193 bits when monitoring frame bit errors. Bit errors other than frame bit errors are not recorded. Frame-bit error monitoring is best used to detect high bit error rates. The longer frame bit errors are monitored, the closer the measured frame-bit error rate approaches the actual bit error rate.

SECTION 5

JITTER MEASUREMENT AND INJECTION

5.1 WHAT IS JITTER?

In digital transmission systems such as T-carrier, digital radio, or fiberoptic transmission systems, signals must contain both data and clock information. Data is encoded in the form of pulses (pulse = 1, no pulse = 0), but clock information is not. Instead, a digital receiver must extract clock information from the incoming digital signal using a frequency-selective (tuned) circuit such as a Phase-Locked Loop (PLL) or tank circuit.

CLOCK RECOVERY must always be performed by a digital receiver so it can read the data contained in the incoming signal (see Figure 7). The recovered clock samples the incoming signal to determine which time slots contain pulses (1's) and which do not contain pulses (i.e., 0's).

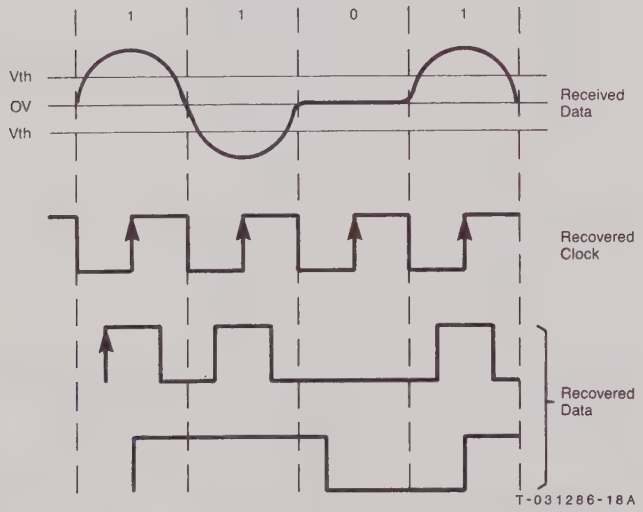

Fig. 7 – Relationship of Clock Signal to Data Bits

Jitter in a digital signal may be defined as short-term variations of the significant instants of a digital signal from their ideal position in time (see Figure 8). The definition of "significant instants" varies depending on the design of the digital system. Significant instants can be interpreted to mean pulse locations, or more specifically, pulse transition locations (i.e., pulse leading- and trailing-edge locations).

Because digital receivers must recover a clock signal from the incoming digital signal, jitter in the incoming signal results in a jittered recovered clock. Recovered-clock jitter may be defined as short-term variations in phase from its long-term average phase.

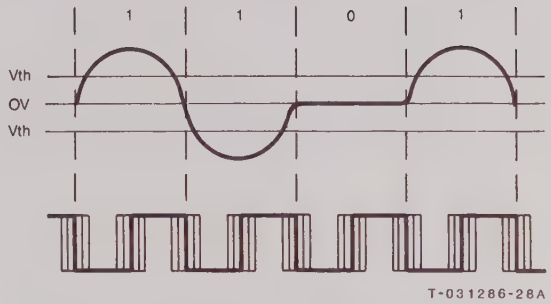

Fig. 8 – Deviation from the Ideal Sampling Point due to Jitter

5.2 UNITS OF JITTER

Jitter is normally expressed in terms of UNIT INTERVALS. One Unit Interval at a given DS rate is equal to one time slot at the DS rate. The values of one Unit Interval at each of the DS rates addressed by the S5104 are listed below:

DS	BIT RATE	UNIT INTERVAL
DS1	1.544 MHz	648 ns
DS1C	3.152 MHz	317 ns
DS2	6.312 MHz	158 ns

Jitter can also be expressed in degrees (i.e., 360° = 1 UI).

5.3 PEAK-TO-PEAK JITTER VS. RMS JITTER

The negative effects of jitter are directly related to PEAK jitter values rather than average or RMS jitter values (see Figure 9). Therefore, jitter specifications are usually ex-

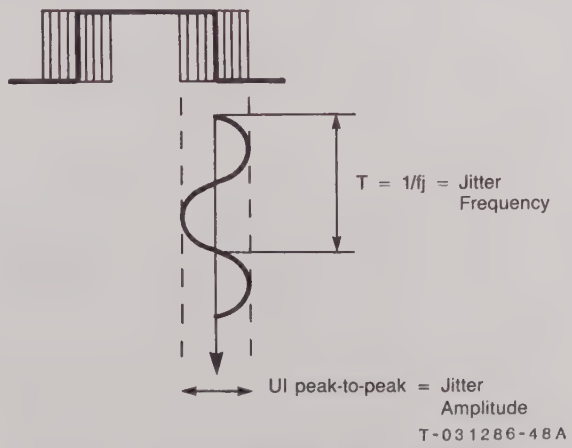

Fig. 9 – Jitter Frequency and Amplitude

pressed in terms of Unit Intervals Peak-to-Peak (UI_{pk-pk}), and jitter measuring instruments are usually equipped with peak detector circuits.

Peak-to-peak jitter, over a given interval, is the difference between the most positive (positive peak) and most negative (negative peak) instantaneous phase detected over the interval. The S5104 measures peak-to-peak, positive-peak, and negative-peak jitter.

5.4 CAUSES OF JITTER

Jitter is caused by a number of sources. The most serious source of jitter in T-carrier networks is pattern-dependent or systematic jitter. T-carrier repeater clock-recovery circuits tend to generate phase lead for certain types of patterns and phase lag for others. Because each repeater tends to act the same way, pattern-dependent jitter in a chain of digital repeaters tends to be additive (coherent) and therefore most severe in long T-carrier systems. Pattern-dependent jitter is called systematic because it is the result of the inherent characteristics of the system, rather than the result of outside influences such as noise.

Noise is another cause of jitter. Jitter resulting from cable crosstalk, central-office impulse noise, etc., is called non-systematic because it is due to influences outside the digital transmission system. Noise-related jitter does not tend to be additive and generally is less of a problem in T-carrier systems than pattern-dependent jitter.

Another major source of jitter is multiplexer Waiting-Time Jitter, an unavoidable byproduct of bit stuffing (and de-stuffing) that must be performed by multiplexes to synchronize multiple asynchronous low-speed signals into a single high-rate signal. An M13 multiplex, for example, introduces waiting-time jitter on the DS1 signals (up to 28) that pass through it.

5.5 NEGATIVE EFFECTS OF JITTER

High-Frequency Jitter

The clock recovery circuits in digital receivers must be designed to tolerate long strings of zeros as well as jitter. A digital receiver with a fast-reacting clock recovery circuit can track high-frequency jitter but is very sensitive to long strings of zeros. Conversely, a digital receiver with a slow-reacting clock recovery circuit can tolerate long strings of zeros but is sensitive to high-frequency jitter.

Every clock recovery circuit is designed with a specific bandwidth. Typically, the bandwidth of a DS1-receiver clock recovery circuit is 8 kHz, which achieves the right balance between jitter tolerance and tolerance to zeros. Jitter in signals below 8 kHz is tracked closely, leading to no degradation in error performance. However, DS1-signal jitter above 8 kHz is not tracked and leads to degraded error performance because the recovered clock can no longer sample the incoming signal at the ideal points (the center of each time slot).

High-frequency jitter for a particular DS rate is defined as jitter above the bandwidth of typical clock recovery circuits used at the DS rate. Excessive high-frequency jitter, usually in the 0.1 to 0.3 UI_{pk-pk} range, results in degraded error performance.

Low-Frequency Jitter and Total Jitter

Low-frequency jitter is jitter within the typical clock recovery bandwidth. Therefore, low-frequency jitter has little effect on digital-receiver error rate. However, total jitter (low-frequency jitter plus high-frequency jitter) can cause serious problems in digital terminal and multiplexer elastic-store buffers, which attempt to compensate for differences in clock frequencies in different parts of the network and the jitter.

Elastic-store buffers are like reservoirs, which store water during periods of high flow and release water during periods of low flow. Elastic-store buffers store extra bits during positive phase variations and release bits during negative phase variations.

However, like any reservoir, digital elastic-store buffers have a limited size and therefore can tolerate only so much jitter (or periods of frequency offset) before overflowing (throwing away data bits) or underflowing (running out of data bits).

Digital terminals can handle overflow or underflow by performing a controlled slip, which at the DS1 rate is the deletion or repetition of one complete 193-bit frame. Slips degrade digital transmission quality (they cause pops and clicks on voice circuits and seriously affect data circuits). Therefore, total jitter must be controlled. Typical network (total) jitter specifications are 5 UI_{pk-pk} maximum.

5.6 JITTER MEASUREMENT FILTERS

Current CCITT and (provisional) Committee-T1 (ANSI accredited) recommendations for digital-network jitter specifications take into account the different effects of total and high-frequency jitter. Their jitter specifications include separate total and high-frequency jitter limits. Both CCITT and Committee-T1 recommendations specify the filters that must be used when measuring jitter. The S5104 is equipped with both total and high-frequency jitter measurement filters

compatible with the current draft recommendations from Committee-T1 at DS1, DS1C, and DS2 rates (see Figure 10).

5.7 HOW TO MEASURE JITTER WITH YOUR S5104

If your S5104 is equipped with the Jitter option, you can perform jitter measurements of DS1, DS1C, and DS2 signals. DS1 and DS1C jitter measurements can be performed on either bipolar or Non Return to Zero (NRZ) signals. However, please note that your S5104 cannot support the measurement of DS2 jitter via the rear-panel BNC NRZ data and clock inputs.

Jitter is measured on bipolar signals input via the front-panel Receiver input jacks or on signals input via the rear-panel BNC NRZ data and clock inputs (see Figure 11). Jitter measurements are made simultaneously with other measurements (i.e., BPV and bit errors). Jitter measurement results can be reviewed during or after a test with the front-panel Receiver MEASUREMENT TYPE and SELECT pushbuttons.

5.8 HOW TO INJECT JITTER FOR JITTER TOLERANCE TESTING

Jitter tolerance (the jitter amplitude tolerated before the onset of errors) is dependent on the jitter frequency. In general, a system can tolerate more jitter at lower frequencies. The same jitter amplitude at different frequencies may have drastically different effects on system performance.

You can deliberately inject jitter into a system with your S5104 to test the system's tolerance to jitter. Set the jitter frequency

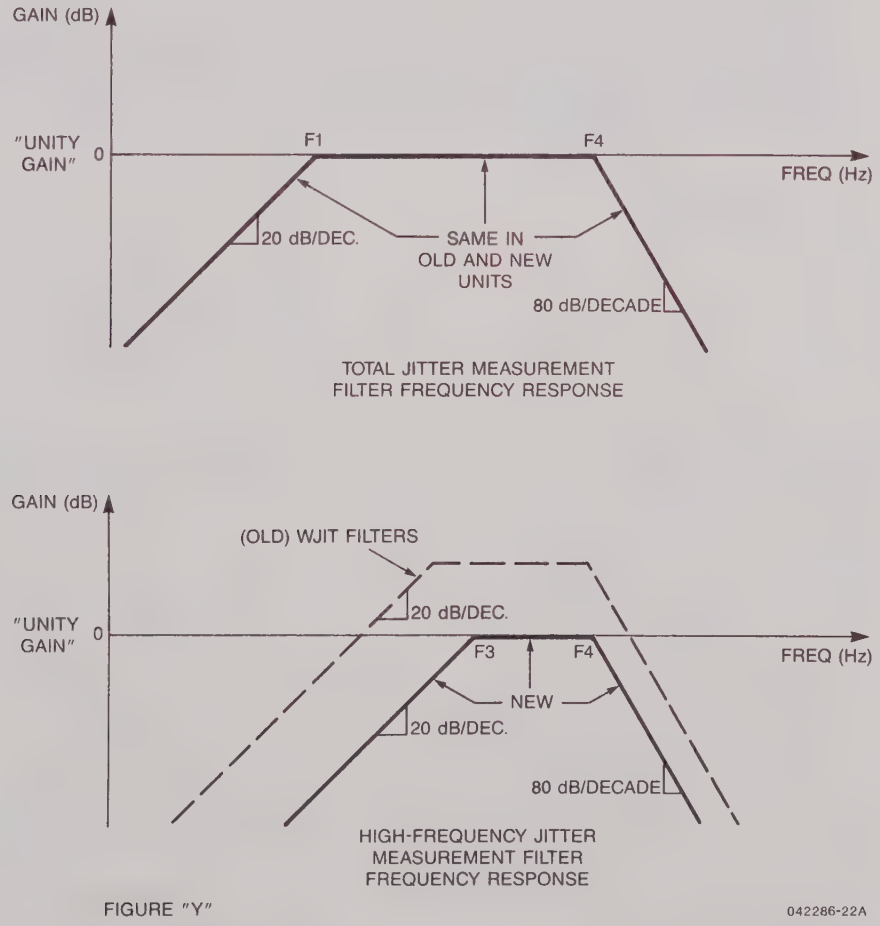

Fig. 10 – S5104 Jitter Measurement Filters

and amplitude of the injected jitter by pressing the front-panel ERROR INJECT JITTER pushbutton. You can also modulate jitter from an external source through the rear-panel JITTER IN BNC connector. This external jitter can then be injected into a signal by the Transmitter.

By increasing the jitter frequency and/or amplitude until the onset of bit errors (if any), you can test a system's jitter tolerance.

BREAK FREQUENCIES OF S5104 JITTER MEASUREMENT FILTERS

DS RATE	F1	F3	F4	
DS1	10 Hz	8 kHz	68 kHz	(See Note 2)
DS1C	10 Hz	2 kHz	135 kHz	(See Note 2)
DS2	10 Hz	3 kHz	270 kHz	(See Note 2)

Note 1 All filters have low-frequency roll-offs of 20 dB per decade (i.e., 1–pole roll-offs) and high-frequency roll-offs of 80 dB per decade (i.e., 4–pole roll-offs).

Note 2 The S5104 *exceeds* T1X1 recommended minimum F4 values of 40 kHz for DS1, DS1C, and DS2 to provide a more useful measurement of high-frequency jitter than the T1X1 specification requires.

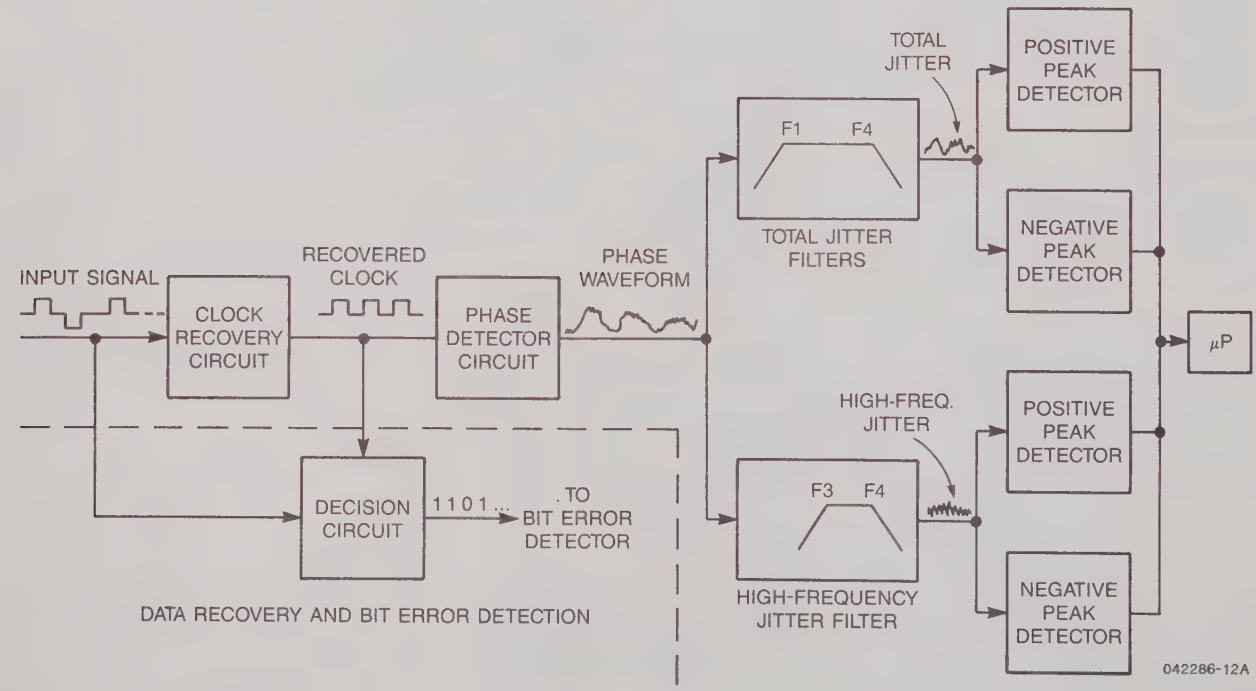

Fig. 11 – How the S5104 Measures Jitter

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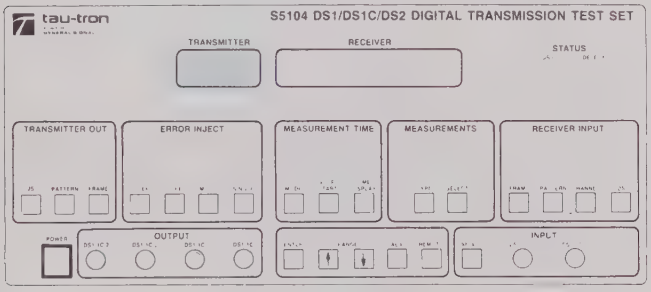
SECTION 1
THE S5104 FRONT PANEL CONTROLS AND INDICATORS

The front panel is divided into two major sections: a **TRANSMITTER** section and a **RECEIVER** section. These sections are further divided into areas of functionally related controls, indicators, and connectors.

1.1 TRANSMITTER OPERATION

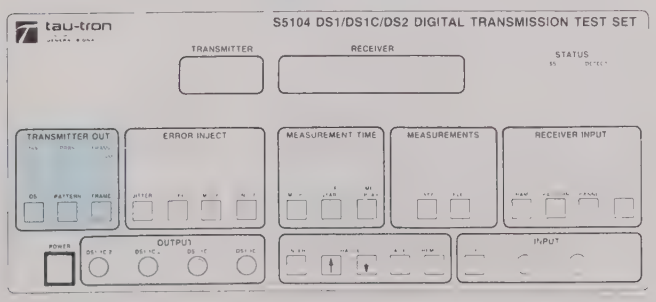
The **TRANSMITTER** section is located on the left side of the front panel. This section contains the output connectors and is used to select the type of signal and errors you wish to transmit.

1.1.1 TRANSMITTER Display



The **TRANSMITTER** display is a 4-character, vacuum-fluorescent, alphanumeric display. You may set and view error rates and jitter parameters on this display.

1.1.2 TRANSMITTER OUT Pushbuttons and Indicators



Use these pushbuttons and indicators to set the type of signal to be generated by the Transmitter.

DS Pushbutton

Press **DS** to select the type of bipolar signal you wish to transmit. The signal to be transmitted is illuminated. The available signals are:

DSX1 — The standard DS1 cross-connect level bipolar signal. The DS1 bit rate is 1.544 Mb/s and the level is ±3 volts peak ±10%.

DSX1C — DS1C cross-connect level bipolar signal. The DS1C bit rate is 3.152 Mb/s and the level is ±3 volts peak ±10%.

DS2H — DS2 High level (nominal rectangular pulse shape) bipolar signal. The DS2 bit rate is 6.312 Mb/s and the High level is ±2.1 volts peak ±0.25 volts.

DSX2 — DS2 cross-connect level bipolar signal. The DS2 bit rate is 6.312 Mb/s, and the DSX2 signal is equivalent to the DS2H signal attenuated by 1000 ft (300m) of ABAM cable.

PATTERN Pushbutton

Press **PATTERN** to select the type of data (bit) pattern you wish to transmit. The selected data pattern is illuminated. There are four data patterns from which to choose:

PRBS — A pseudorandom bit sequence with a bit length of $2^{20}-1$ (1,048,575) bits. There is no synchronization between the PRBS and frame bits in a framed signal. Frame bits are gapped into the bit pattern and do not overwrite bits in the PRBS. The DS1 PRBS has a 14-zero constraint.

FIXED — A repeating bit pattern with a length of 16 to 24 bits. The exact pattern and bit length is set by the **PROGRAMMABLE FIXED WORD** DIP switches on the rear panel of your S5104. There is no synchronization between the FIXED bit pattern and the frame bits in a framed signal. Frame bits are gapped into the bit pattern and do not overwrite bits in the FIXED bit pattern.

ALL 1's A bit pattern in which all the transmitted bits are 1's. An UNFRAMED ALL 1's pattern is also known as an Alarm Indication Signal (AIS) at the DS1, DS1C, and DS2 rates.

THRU Press **THRU** when you want to add errors or jitter to live traffic. The recovered clock and data bits from a received signal are automatically routed internally to the S5104 Transmitter. Errors and/or jitter may then be injected into the signal. Transmitter **FRAME** and **DS** settings are slaved to the Receiver **FRAME** and **DS** settings. Therefore, the Receiver **FRAME** and **DS** levels you select are selected automatically for the Transmitter. The S5104 ignores the Transmitter **FRAME** and **DS** pushbuttons when the Transmitter is set to **THRU**.

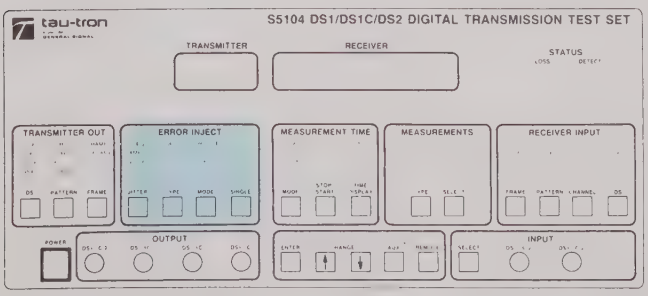
FRAME Pushbutton

Press **FRAME** to select either framed or unframed data pattern to be transmitted.

FRAME The frame bits are gapped into the data pattern and do not overwrite other data bits.

UNFRAME No frame bits are inserted into the data pattern.

1.1.3 ERROR INJECT Pushbuttons and Indicators



Use these pushbuttons and indicators to select and set the types of errors and /or jitter to be injected into the transmitted signal.

JITTER Pushbuttons

Press **JITTER** to select one of the four available jitter parameters: Frequency, Amplitude, Internal Jitter Injection, or External Jitter Injection. If your S5104 does not have the Jitter Option, the **TRANSMITTER** display shows **N/A** (not available) when you press this pushbutton. The green indicator above the **JITTER** pushbutton lights when jitter data is displayed on the **TRANSMITTER** display. For a complete description of jitter frequency and amplitude, refer to Jitter Injection and Measurement at the end of this section.

FREQ When first lit, the current jitter frequency value appears on the **TRANSMITTER** display. If you wish to change the value, press **JITTER**. This initiates the edit procedure, and the leftmost digit in the display flashes. You may change the value of a flashing digit with the front-panel **CHANGE** pushbuttons located on the Receiver-side of your S5104. Once the desired value is displayed, press **ENTER** to save the digit. The **ENTER** pushbutton is located to the left of the **CHANGE** pushbuttons. Repeat this procedure for the remaining digits. The jitter frequency value is saved when the last digit is entered.

Jitter frequency is displayed in units of hertz. The units are displayed in scientific notation in the format A.BC,X. A.BC is a number between 1.00 and 9.95, and X is the power-of-ten exponent. For example, if the display shows 2.50,4, the jitter frequency to be transmitted is 25,000 hertz or 25 kHz.

The maximum allowable jitter-generation frequencies are as follows:

- DS1 40 kHz
- DS1C 80 kHz
- DS2 160 kHz

If you try to enter an invalid jitter frequency value, you are alerted with an error message on the **TRANSMITTER** display. The display reads **HIGH** and the previous frequency does not change. Pressing **ENTER**

again puts the left-most digit back into the edit mode.

AMPL When first lit, the current jitter amplitude value appears on the **TRANSMITTER** display. You may change the jitter amplitude value using the editing procedure described previously for jitter **FREQ**. If the amplitude is too high for the frequency, the display reads **HIGH** and the value does not change. The jitter specifications in SECTION 9 show the maximum jitter the 5104 can generate as a function of DS rate and jitter frequency.

Jitter amplitude is displayed in Unit Intervals (UI). The display format for jitter amplitude is XX.XX where XX.XX is the 4-digit amplitude value.

INT When lit, the Transmitter is set for internal jitter injection (internal jitter is **ON**). When this indicator is initially selected, it flashes and the word **ON** in the **TRANSMITTER** display flashes. If you press the front-panel **ENTER** pushbutton at this time, internal jitter is set to **ON**. To turn **OFF** internal jitter, press one of the front-panel **CHANGE** pushbuttons to show the word **OFF** in the display; then press **ENTER**.

EXT This lights when the Transmitter is set for external jitter injection. External jitter is turned **ON** and **OFF** in the same manner as described for **INT** jitter injection. The signal to input external jitter to the Transmitter is applied to the rear-panel **TRANSMITTER JITTER IN** BNC connector. This signal is used to modulate the Transmitter clock and data. When external jitter is **ON**, you may program (edit) jitter amplitude, but the jitter frequency may not be edited.

TYPE Pushbutton

Press **TYPE** to select the type of errors you wish to inject into the transmitted signal; either bit errors or BPV's.

BIT If lit, bit errors are injected into the Transmitter signal when the Transmitter is set for internal error injection. For framed signals, bit errors are inserted in *both* data bits and frame bits.

BPV When lit, bipolar violations are injected into the Transmitter signal when the Transmitter is set for internal error injection.

MODE Pushbutton

Press **MODE** to set the mode and rate of error injection. When error-rate data is displayed in the **TRANSMITTER** display, the indicator above the **MODE** pushbutton lights.

ERR FREE When lit, the Transmitter transmits signals without injecting errors into the signal.

INT When lit, the Transmitter is set to inject either **BIT** errors or **BPV**'s at the rate shown in the **TRANSMITTER** display.

This indicator flashes when you first select it; the leftmost digit in the **TRANSMITTER** display also flashes. This is an edit condition prompting you to enter or edit the digit flashing in the display. The value in the display is the error-rate value represented in scientific notation. The format is XE–Y, where X is an integer from 1 to 9 and Y is the exponent and an integer from 3 to 8. E– is symbolic for a power-of-ten notation. For example, if 2E–5 is shown on the display, it represents an error rate of 2×10^{-5}. Put more simply, two errors are injected out of every 100,000 bits. The range of the error injection rate is from 9×10^{-3} to 1×10^{-8}.

Press **CHANGE** to alter the value of the integer flashing in the display. Once the desired integer is displayed, press **ENTER** to insert the integer. The **INT** indicator and the display stop flashing after you have entered the exponent.

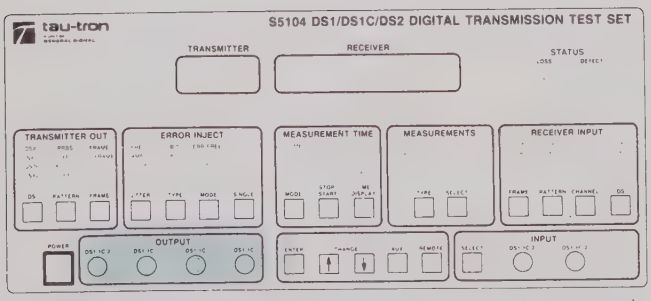
EXT Bit errors or BPV's may be injected into the Transmitter signal from an external source. The signal containing the errors is applied to the rear-panel **TRANSMITTER EXT ERR** BNC connector. When **EXT** is lit, the Transmitter accepts the errors from the applied signal and injects them into the Transmitter signal.

The S5104 measures externally injected error rate averaged over 1×10^7 transmitted bits. The calculated external error rate is displayed in the **TRANSMITTER** display in the format n.n–x, where n.n is a number between 0.0 and 9.9 and x is the exponent of the base 10. Therefore, if 1.2–5 appears in the display, it represents an error rate of 1.2×10^{-5} or 12 errors out of every million bits.

SINGLE Pushbutton

Press **SINGLE** to inject a single bit error or BPV. Select the type of error by pressing the **TYPE** pushbutton, which is only operational when the Transmitter is set for **ERR FREE** operation. Framing bits are not errored by the **SINGLE** error. Single bit errors cannot be injected in the **THRU** mode.

1.1.4 OUTPUT Jacks

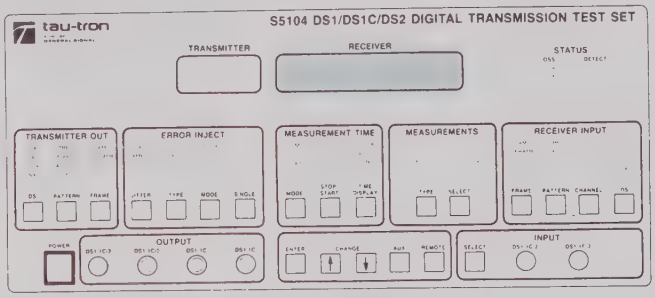


These four jacks output the signal generated by the Transmitter. The jacks accept WECo 310-type plugs. You may use all four simultaneously. The two leftmost jacks labeled **DS1/1C/2** are capable of outputting all DS signal levels. The other two labeled **DS1/1C** are only capable of outputting DS1 and DS1C signals.

1.2 RECEIVER OPERATION

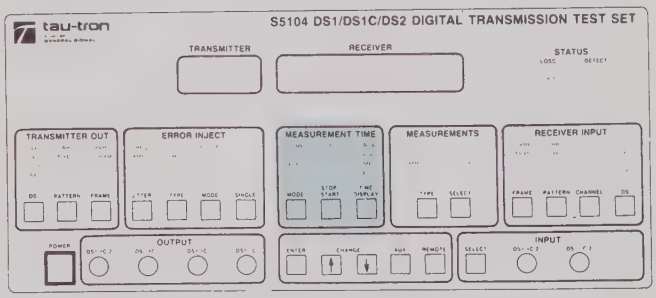
The **RECEIVER** section is located on the right side of the front panel. This section contains the input connectors and is used to set measurement parameters through the use of pushbuttons and their associated indicators.

1.2.1 RECEIVER Display



The **RECEIVER** display is a 10-character, vacuum-flourescent, alphanumeric display. This display shows measurements and time and date, and scrolls error messages when invalid parameters are programmed.

1.2.2 MEASUREMENT TIME Pushbuttons and Indicators



Use these pushbuttons and indicators to set and display test measurement times, to set the time of day and date, and to start and stop tests.

MODE Pushbutton

Press **MODE** to select the interval of time you wish a test to run. There are three test time intervals from which to choose: **UNTIMED**, **SINGLE**, and **REPEAT**.

UNTIMED When lit, a test runs continuously until it is interrupted or stopped (by pressing the **STOP/START** pushbutton).

SINGLE When lit, a test runs for a period of time programmed with the **TIME DISPLAY** pushbutton. In this mode, a test runs once and holds the measurement results until you select or start another test. You can program tests to run from 1 second up to 100 days.

REPEAT This mode operates like the **SINGLE** mode described above. However, at the completion of the test interval, the test restarts and repeats. Test results are held at the end of each test interval. You may review the results of the most recently completed test on the **RECEIVER** display by pressing **AUX** and selecting **RECALL**.

STOP/START Pushbutton

Press **STOP/START** to start and stop tests.

IN PROC Lights when a test is started and remains lit while the test is in process.

STOP SET Flashes when a test is stopped. A test that is stopped cannot be continued. The test must be restarted with the **STOP/START** pushbutton. A test that is stopped with the **STOP/START** pushbutton is shown on the **RECEIVER** display. You may review the results of the test by pressing **AUX** to access **RECALL**.

TIME DISPLAY Pushbutton

Press **TIME DISPLAY** to select the type of time you wish to view or set. This includes real-time and date settings as well as test interval settings.

INTRVAL When lit, the period of time a test is set to run appears in the **RECEIVER** display. The test interval is displayed in the format:

DD-HHMM:SS

DD is the number of days, from 0 to 99. HH is the number of hours, from 0 to 23. MM is the number of minutes, from 0 to 59. SS is the number of seconds, from 0 to 59.

To change the time of the test interval, press **TIME DISPLAY** when the **STOP SET** indicator is flashing and the **INTRVAL** indicator is lit. This causes the ten's digit for the days to flash. You may save the flashing number by pressing **ENTER** or change the number by pressing **CHANGE**. Once the desired number is shown, save it by pressing **ENTER**; the indicator will stop flashing. Continue editing in the same manner until all numbers have been entered.

ELAPSED When lit, the time that has elapsed since a test was started appears in the **RECEIVER** display. This time is displayed in the same format as the test interval time described above.

TIME When lit, the time of day is shown in the **RECEIVER** display. The time is displayed as a 24-hour clock in the following format:

HHMM:SS

HH is the hour, from 0 to 23. MM is the minutes, from 0 to 59. SS is the seconds, from 0 to 59.

Batteries inside your S5104 maintain the clock while the unit is not on and last for several months when fully charged.

To reset the time, press **TIME DISPLAY** when the **STOP RESET** indicator is flashing and the **TIME** indicator is lit. This causes the **TIME** indicator and the leftmost digit in the display to flash. You may save the flashing digit by pressing **ENTER** or change it by pressing **CHANGE**. When the desired number is displayed, save it by pressing **ENTER**. Continue this procedure for the remaining digits in the display.

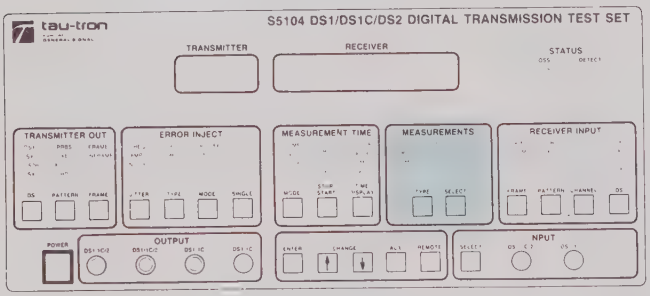
DATE When lit, the current date appears in the **RECEIVER** display in the following format:

DD-MMM-YY

DD is the day. MMM is the month represented as a three-letter abbreviation. YY is the year.

To change the date, press **TIME DISPLAY** when the **STOP SET** indicator is flashing and the **DATE** indicator is lit. This causes the **DATE** indicator and the leftmost digit in the display to flash. Edit the display in the same manner as previously described for **TIME**.

1.2.3 MEASUREMENTS Pushbuttons, Indicators, and Displays



Use these pushbuttons and indicators to select the type of measurement you wish to display in the **RECEIVER** display and to review measurement results. All measurements are made simultaneously. However, bit and frame measurements are not simultaneously detected because they share common hardware and software.

NOTE: Be sure to select either* BIT *or* FRAME *prior to the start of your test.

TYPE Pushbutton

Press **TYPE** to select the general type of measurement you wish to see. If you select a measurement that is invalid for the current Transmitter and/or Receiver settings, an error message scrolls across the **RECEIVER** display to inform you of the problem.

BIT Lights when you select bit error measurements for review. Bit error measurements cannot be made for live traffic measurements.

BPV Lights when you select BPV measurements for review.

FRAME Lights when you select frame error measurements for review. Frame error measurements are made for live traffic measurements only.

STATUS Lights when you select status event seconds for review. A status event second is a second in which the S5104 detects the occurrence of one or more of the following events:

- Loss of signal
- Loss of frame
- Loss of synchronization
- Detection of excess 0's
- Detection of excess 1's
- Detection of an X-bit

JITTER Lights when you select jitter measurements for review.

RECALL Flashes when you press **AUX** to turn **ON** the **RECALL** function. This causes the **RECEIVER** display to show the measurement results from the previously completed test for each measurement type. The **RECALL** indicator remains flashing until **RECALL** is turned **OFF**. All current measurements are still accumulated.

SELECT Pushbutton

Press **SELECT** to scroll through and review the measurement results for the measurement type you selected. Measurement results are shown on the **RECEIVER** display. The available measurements for each measurement type are as follows:

BIT and **BPV** Measurements

ERRORS (TOTAL)

Display format: nnnnnnn**TOT**

The total number of accumulated errors since the start of the test. The error range is from 0 to 9,999,999.

AVERAGE ERROR RATE

Display format: n.nE–x**AVG**

The average error rate for the test period, represented in scientific notation; n.n is a number between 0.0 and

9.9 and x is the exponent. For example, if 1.2E-5 appears in the display, it represents an average error rate of 1.2×10^{-5} or 1.2 errors out of every 100,000 bits.

ERRORED SECONDS (TOTAL)

Display format: nnnnnn**ESEC**

The total number of errored seconds during the test. The number of errored seconds recorded can be from 0 to 999,000.

ERRORED SECONDS (ERROR RATE $> 10^{-5}$)

Display format: nnnnnn**E-5**

The number of synchronous errored seconds during the test in which the error rate exceeded 1×10^{-5}.

ERRORED SECONDS (ERROR RATE $> 10^{-4}$)

Display format: nnnnnn**E-4**

The number of synchronous errored seconds during the test in which the error rate exceeded 1×10^{-4}.

ERRORED SECONDS (ERROR RATE $> 10^{-3}$)

Display format: nnnnnn**E-3**

The number of synchronous errored seconds during the test in which the error rate exceeded 1×10^{-3}.

ERRORS (DRIBBLING)

Display format: nnnnnnn**DRB**

The total number of dribbling errors that occurred during the test. Dribbling errors are errors that occur during seconds in which the error rate is $< 10^{-6}$.

NOTE: For DSI this means all seconds with one and only one error.

% ERROR FREE SECONDS

Display format: nnn.nnn**%EF**

The percentage of seconds that no errors occurred during the test.

FRAME Measurements

FRAME BIT ERRORS (TOTAL)

Display format: nnnnnnn**TOT**

The total number of frame errors that occurred during the test.

FRAME BIT AVERAGE ERROR RATE

Display format: n.nE-xx**AVG**

The average frame bit error rate displayed in scientific notation; n.n is a number between 0.0 and 9.9 and xx is the exponent. For example, if 1.2E-10 appears in the display, it represents a frame bit error rate of 1.2×10^{-10}.

FRAME BIT ERRORED SECONDS

Display format: nnnnnn**ESEC**

The total number of synchronous errored seconds that contained frame bit errors during the test.

% FRAME BIT ERROR FREE SECONDS

Display format: nnn.nnn**%EF**

The percentage of seconds during the test that no frame bit errors occurred.

STATUS Measurements

SIGNAL LOSS SECONDS

Display format: nnnnnn**SGLS**

The number of seconds in which the S5104 detected a loss of signal. A signal is considered lost when no bipolar pulses are detected in a 25-microsecond period.

FRAME LOSS SECONDS

Display format: nnnnnn**FRAM**

The number of seconds that framing was lost during the test. Frame is considered lost when three out of six frame bits are in error. Frame is considered regained when ten consecutive correct frame bits are detected.

(PATTERN) SYNC LOSS SECONDS

Display format: nnnnnn**SYNC**

The number of seconds that data synchronization was lost during the test. If 12 bit errors are detected in a 40-bit block, data synchronization is considered lost. When 40 consecutive error-free bits are detected, sync is regained.

EXCESS ZEROS SECONDS

Display format: nnnnnn**ZERO**

The number of seconds that excess 0's were detected in the bipolar signal during the test. The number of consecutive 0's required to cause an excess 0's condition is as follows:

- DS1 AMI — 16 or more
- DS1 B8ZS — 8 or more
- DS1C — 34 or more
- DS2 — 6 or more

ALL 1's SECONDS

Display format: nnnnnn**ONES**

The number of seconds that excess 1's were detected during the test. The number of consecutive 1's required to cause an excess 1's condition is as follows:

- DS1 framed/unframed 1,000 ± 200
- DS1C framed 1,000 ± 200
- DS1C unframed 2,000 ± 200
- DS2 framed 1,000 ± 200
- DS2 unframed 4,000 ± 200

X-BIT SECONDS

Display format: nnnnnn**XBIT**

The number of seconds that X-bits were detected during the test. X-bits are detected at logic 0 for DS1C and DS2 only.

JITTER Measurements

NOTE: ALL jitter measurements are expressed in UNIT INTERVALS.

CURRENT JITTER AMPLITUDE (PK–PK)

Display format: nn.nn**JCUR**

The current jitter amplitude measured in unit intervals; nn.nn is the number of unit intervals.

MAXIMUM PEAK-TO-PEAK JITTER AMPLITUDE

Display format: nn.nn**JMAX**

The maximum jitter amplitude during the test period measured in unit intervals.

CURRENT POSITIVE PEAK JITTER AMPLITUDE (PK)

Display format: nn.nn**J+PKCU**

The current +peak jitter amplitude measured in unit intervals.

MAXIMUM POSITIVE PEAK JITTER AMPLITUDE (PK)

Display format: nn.nn**J+PKMX**

The maximum +peak jitter amplitude that occurred during the test period.

CURRENT NEGATIVE PEAK JITTER AMPLITUDE (PK)

Display format: nn.nn**J−PKCU**

The current −peak jitter amplitude measured in unit intervals.

MAXIMUM NEGATIVE PEAK JITTER AMPLITUDE (PK)

Display format: nn.nn**J−PKMX**

The maximum −peak jitter amplitude that occurred during the test period.

CURRENT HIGH-FREQUENCY JITTER AMPLITUDE (PK-PK)

Display format: nn.nn**HJCUR**

The current high-frequency, peak-to-peak jitter amplitude.

MAXIMUM HIGH-FREQUENCY JITTER AMPLITUDE (PK)

Display format: nn.nn**HJMAX**

The maximum high-frequency jitter amplitude that occurred during the test period.

JITTER HIT-SECOND THRESHOLD

Display format: nn.nn**J_THR**

This setting determines the level at which jitter threshold hit seconds will be recorded. Any second in which jitter equals or exceeds this threshold is recorded as a jitter threshold hit second.

When the **STOP SET** indicator is flashing and you select this display, the **J_THR** part of the display flashes. This is an edit prompt. If you wish to select unit interval threshold seconds to be measured, press **ENTER**. The leftmost integer in the display now flashes. Either save the flashing value by pressing **ENTER**, or change the value by pressing the **CHANGE** pushbuttons and then pressing **ENTER**. Continue this procedure for the remaining integers. After you enter the last integer, the unit interval threshold is set for the value you selected.

HIGH-FREQUENCY JITTER HIT-SECOND THRESHOLD

Display format: nn.nn**HJ_THR**

Determines the level at which high-frequency jitter hit seconds will be recorded. Any second in which the high-frequency jitter number equals or exceeds this threshold number is recorded as a high-frequency jitter threshold hit second.

When the **STOP SET** indicator is flashing, the **HJ_THR** part of the display flashes and high-frequency jitter threshold may be selected and edited, as described above

for Jitter Hit-Second Threshold settings. To access the high-frequency jitter threshold display, press one of the **CHANGE** pushbuttons when the **J_THR** display is flashing. This switches the display from jitter threshold to high-frequency jitter threshold.

You may select either the high-frequency jitter threshold or the jitter threshold. However, you may use only *one* threshold during a test.

JITTER HIT SECONDS

Display format: nnnnnn**JHS**

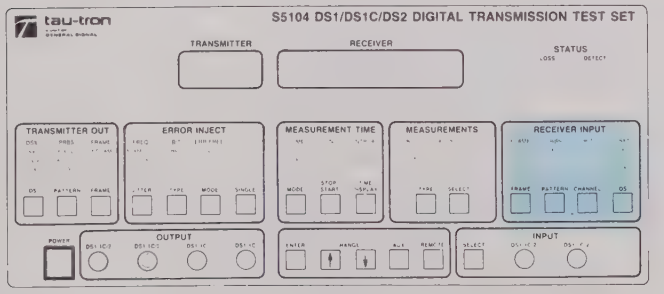
The number of seconds (hit seconds) in which the jitter amplitude (PK-PK) equaled or exceeded the value set for the Jitter Hit-Second Threshold. Up to 999,999 jitter hit seconds may be recorded. If the number of hit seconds exceeds this number, the five least significant digits are shown, preceded by a flashing '*' (*nnnnn**JHS**). This is an overflow indication.

HIGH-FREQUENCY JITTER HIT SECONDS

Display format: nnnnnn**HJHS**

The number of seconds in which the high-frequency jitter (PK-PK) equaled or exceeded the value set for the high-frequency jitter threshold. Up to 999,999 high-frequency jitter hit seconds may be recorded. If the number of hit seconds exceeds this number, the five least significant digits are shown, preceded by a flashing '*' (*nnnnn**HJHS**). This is an overflow indication.

1.2.4 RECEIVER INPUT Pushbuttons and Indicators



Use these pushbuttons and indicators to set the Receiver for the expected input signal.

FRAME Pushbutton

Press **FRAME** to select framed or unframed signals to be input into the Receiver. If a framed signal is input to the Receiver, the Receiver should be set for **FRAME**.

FRAME — When lit, the Receiver is set to accept signals with framed data patterns.

UNFRAMED — When lit, the Receiver is set to accept signals with unframed data patterns.

PATTERN Pushbutton

Press **PATTERN** to select the data pattern expected for input to the Receiver.

PRBS — When lit, the **PRBS** data pattern is selected as the data pattern expected for input to the Receiver. PRBS stands for pseudorandom bit sequence and is a repeating bit pattern of $2^{20}-1$ (1,048,575) bits. DS1 PRBS has a 14-zero constraint. There is no synchronization between the PRBS and frame bits in a framed signal. Frame bits are gapped into the bit pattern and do not overwrite bits in the PRBS.

FIXED — When lit, the **FIXED** data pattern is selected as the data pattern expected for input to the Receiver. The FIXED data pattern is generated by the S5104 Transmitter and is a repeating bit pattern of 16 to 24 bits. There is no synchronization between the FIXED bit pattern and frame bits in a framed signal. Frame bits are gapped into the bit pattern and do not overwrite bits in the FIXED bit pattern.

LIVE — When lit, **LIVE** traffic is selected as the expected input to the Receiver.

CHANNEL Pushbutton

Press **CHANNEL** to select a channel from the input signal. A channel can be thought of as a DS1 signal. A DS1C signal is two multiplexed DS1 signals, and a DS2 signal is four multiplexed DS1 signals. Therefore, a DS1C signal has two channels, a DS2 signal has four channels, and a DS1 signal is a single channel.

Channels cannot be selected for unframed signals or live traffic. For DS1 signals, select only channel one (**CH1**). You may

select either channel one or two (**CH1** or **CH2**) for DS1C signals, and any of the four available channels for DS2 signals.

Channels are selected to perform error measurements on a single DS1 channel. The only way to do bit error measurements on the entire DS1C or DS2 signal is in the **UNFRAMED** mode.

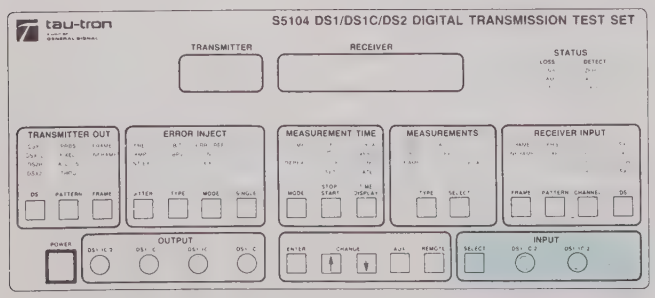
CH 1	Lights when channel one is selected.
CH 2	Lights when channel two is selected.
CH 3	Lights when channel three is selected.
CH 4	Lights when channel four is selected.

DS Pushbutton

Press **DS** to select the bipolar signal level expected for input to the Receiver.

DSX1	The standard DS1 bipolar signal. The DS1 bit rate is 1.544 Mb/s and the level may range between the nominal DSX1 cross-connect level (3 Vpk) or the DSX1 monitor level.
DSX1C	A DS1C bipolar signal. The DS1C bit rate is 3.152 Mb/s and the level may range between the nominal DSX1C cross-connect level (3 Vpk) or the DSX1C monitor level.
DS2H	A DS2 High undisturbed bipolar signal. The DS2 bit rate is 6.312 Mb/s and the High level is ± 2.1 volts ± 0.25 volts.
DSX2	A DS2 bipolar signal. The DS2 bit rate is 6.312 Mb/s and the DSX2 signal is equivalent to the DS2H signal attenuated by 1000 ft (300m) of ABAM cable.

1.2.5 INPUT Jacks



These jacks accept the signal for input to the Receiver.

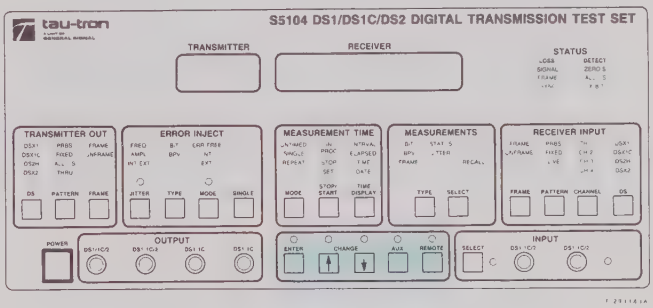
SELECT Pushbutton

Press **SELECT** to select which of the two Receiver input jacks is to be used. *Only one input jack may be used at a time.* The indicator adjacent to the active jack lights.

DS1/1C/2 Jacks

These jacks accept standard WECo 310-type plugs.

1.2.6 Editing and Auxiliary Control and Displays



Use these pushbuttons and indicators to edit information in the **TRANSMITTER** and **RECEIVER** displays and to select auxiliary functions. The indicator above the pushbuttons that are currently active lights.

ENTER Pushbutton

Press **ENTER** to enter and save information that is prompted for editing in the displays.

CHANGE Pushbuttons (↑UP/↓DOWN ARROWS)

Use these pushbuttons to edit values that are prompted for editing in the displays.

AUX Pushbutton

Press **AUX** to select auxiliary functions which will appear in the **RECEIVER** display. The functions are as follows:

PRINTER?	Press the **ENTER** pushbutton to review or change the current printer settings. These settings determine the type of printout. After you select **PRINTER?**, the display shows one of three settings listed below. To select a setting, press the **ENTER** pushbutton. If you wish to change to another setting, press the **CHANGE** pushbuttons to reach your desired setting.

PRINT OFF

Disables the printer; no printouts will be produced.

PRINT BIT

If you enter this selection, an **END OF INTERVAL BIT SUMMARY** is printed at the end of a test. After entering **PRINT BIT**, the display prompts you to enable or disable errored-second printouts (**ERRSEC ON** or **OFF**). An errored-second printout is a line of data which is printed when errors occur in a second during a test.

If you enter **ERRSEC ON**, the display prompts you to enable or disable errored-second squelching, which is used to stop errored-second printouts. When ten consecutive errored seconds occur in which the error rate is at or above the squelch setting, the S5104 stops (squelches) errored-second printouts. **SQU ON ANY** stops errored-second printouts if any errors in a second occur for ten consecutive seconds. **SQU ON E–3**, **SQU ON E–4**, and **SQU ON E–5** stop errored-second printouts when ten consecutive errored seconds occur in which the error rate exceeds 1×10^{-3}, 1×10^{-4}, and 1×10^{-5} respectively.

PRINT BPV

An **END OF INTERVAL BPV SUMMARY** is printed if you enter this selection. Select for errored-second printouts and squelching as described above for **PRINT BIT**.

SNAPSHOT? Press **ENTER** when **SNAPSHOT?** is displayed to print out an **IMMEDIATE BIT** or **BPV SUMMARY**. The type of summary printout (**BIT** or **BPV**) is determined by the **PRINTER?** settings described above. For example, if **PRINT BIT** is selected, an **IMMEDIATE BIT SUMMARY** is printed when **SNAPSHOT?** is entered.

RECALL? Use **RECALL** to review the results of the previous test. Press **ENTER** when **RECALL?** is displayed and press the **CHANGE** pushbuttons to toggle between **ON** and **OFF**. If **RECALL ON** is entered, the **RECALL** indicator on the front panel flashes. When this indicator lights, the **RECEIVER** display shows measurement results from the last completed or stopped test.

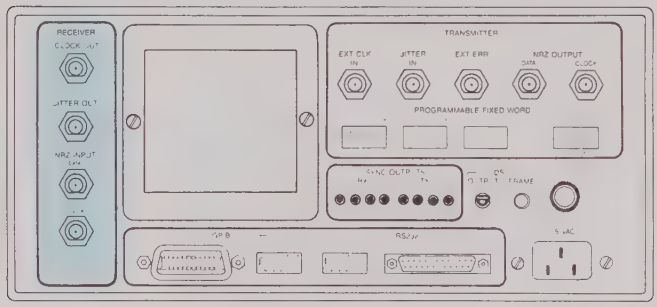
REMOTE Pushbutton

Press **REMOTE** to disconnect the S5104 from GPIB remote control if the GPIB LLO (Local Lockout) command is not active. The indicator above the **REMOTE** pushbutton lights when the S5104 is placed under remote control via the GPIB only.

SECTION 2
THE S5104 REAR PANEL CONNECTORS AND SWITCHES

Contains **TRANSMITTER** and **RECEIVER** I/O BNC connectors, DIP switches to program short data patterns, test points to monitor SYNC OUTPUTS, a DS1 bipolar (AMI)/B8ZS toggle switch, and GPIB and RS-232C Interface connectors. In addition, a fan and an AC power connector are located on the rear panel.

2.1 RECEIVER CONNECTORS



032185-11A

BNC connectors. Input NRZ clock and data signals or output clock and/or jitter.

CLOCK OUT

BNC connector. Outputs TTL-compatible (logic 0 = 0.2 to 0.4 volts, logic 1 = 2.4 to 5 volts) recovered clock from the input data stream. Capable of driving 75 ohms and 10 feet (3 meters) of cable.

JITTER OUT

BNC connector. Capable of driving 75 ohms, DC-coupled output. Outputs demodulated jitter from the Receiver in all modes except external jitter. Maximum jitter output is 11 Unit Intervals (UI) peak-to-peak. 0.8 volts peak-to-peak per unit interval. 8.8 volts peak-to-peak maximum.

NRZ INPUT

BNC connectors. Input an NRZ (Non-Return to Zero) unipolar binary signal.

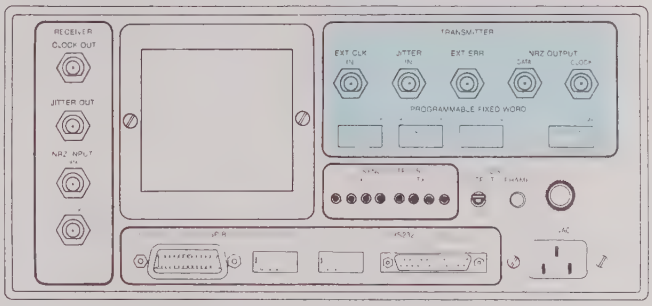
DATA

BNC connector. Accepts TTL-compatible data input signals. Bypasses bipolar decoding and timing recovery. Accepts 75-ohm impedance.

CLOCK

BNC connector. Accepts TTL-compatible clock input signals and 75-ohm impedance. The positive clock edge in the center of the data bit can be changed 180° by an internal jumper. Bypasses bipolar decoding and timing recovery. Frequency range is 1 to 7 MHz. Pulse width is one-half the clock period. When an external clock signal is applied, the signal overrides and takes precedence over the internal clock. Bipolar inputs are ignored.

2.2 TRANSMITTER CONNECTORS AND DIP SWITCHES



032185-11A

BNC connectors. Input/output signals to and from the Transmitter. **PROGRAMMABLE FIXED WORD** DIP switches for setting short fixed-data patterns.

EXT CLK IN

BNC connector. Inputs TTL-compatible signals with 75-ohm impedance. Accepts a clock range of 1 to 7 MHz. When an external clock signal is applied to this connector, the signal overrides and takes precedence over the internal clock.

JITTER IN

BNC connector. Accepts 600-ohm nominal input impedance to input jitter from an external source to the Transmitter. When the Transmitter is set for external jitter, applying an external modulating input (jitter) adds timing jitter to the Transmitter **NRZ CLOCK/DATA** and bipolar DS1, DS1C, and DS2 signals. 0.8 volts peak-to-peak per Unit Interval (UI).

EXT ERR

BNC connector. Accepts an AC-coupled, 600-ohm nominal input. Use this connector to inject bit errors and BPV's from an external source into the Transmitter's signal. Press the front-panel **ERROR INJECT TYPE** pushbutton to select the type of error to be injected: either **BIT** or **BPV**. To select external error injection, press the **ERROR INJECT MODE** pushbutton to light the **EXT** indicator. Error rates from 10^{-2} to 10^{-8} can be used. The error rate is directly equal to the external error frequency and is displayed on the **TRANSMITTER** display in the external error mode.

NRZ OUTPUT

BNC connectors. Transmitter NRZ Clock and Data outputs. May be used in parallel with bipolar (front panel) outputs.

DATA

BNC connector. TTL-compatible data output signal capable of driving 75 ohms and 10 feet (3 meters) of cable.

CLOCK

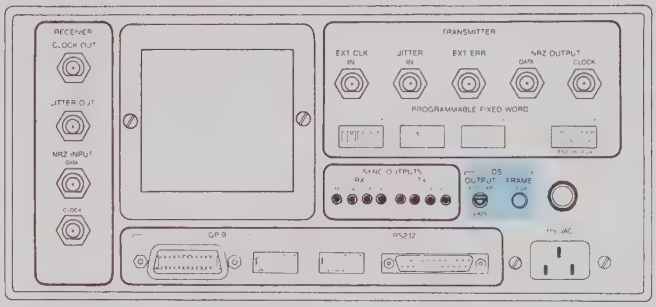
BNC connector. TTL-compatible clock output signal capable of driving 75 ohms and 10 feet (3 meters) of cable. The positive clock edge in the center of the data bit can be changed 180° by an internal jumper. Pulse width is one-half the clock period.

PROGRAMMABLE FIXED WORD

Four DIP switches. Used to set a 16- to 24-bit fixed pattern. The DIP-switch settings determine the fixed pattern to be transmitted when you select **FIXED PATTERN** on the front panel. Switch settings determine the bit value. Set the switch ON (up) for a 1 bit or down (off) for a 0 bit.

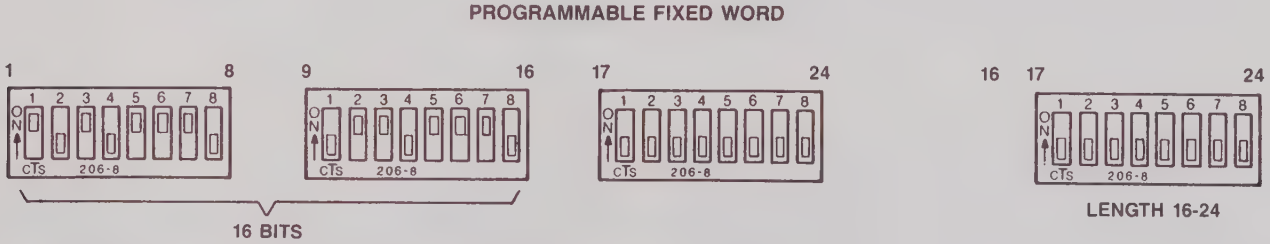
The minimum fixed bit pattern is 16 bits. Therefore, the first 16 switch settings are always read by the S5104 (DIP switches **1–8** and **9–16**). Bit patterns up to 24 bits are programmed with the **17–24** DIP switches. The DIP switches labeled **LENGTH 16–24** must be set for the intended bit length. For a 16-bit pattern, all the switches are set to off (down). For bit patterns from 17 to 24 bits, set **ON** (up) the switch which corresponds to the desired bit length. If more than one switch is **ON**, the bit length is set to the lowest value. Figure 12 shows examples of **PROGRAMMABLE FIXED WORD** settings.

2.3 DS1 OUTPUT BIPOLAR/B8ZS TOGGLE SWITCH

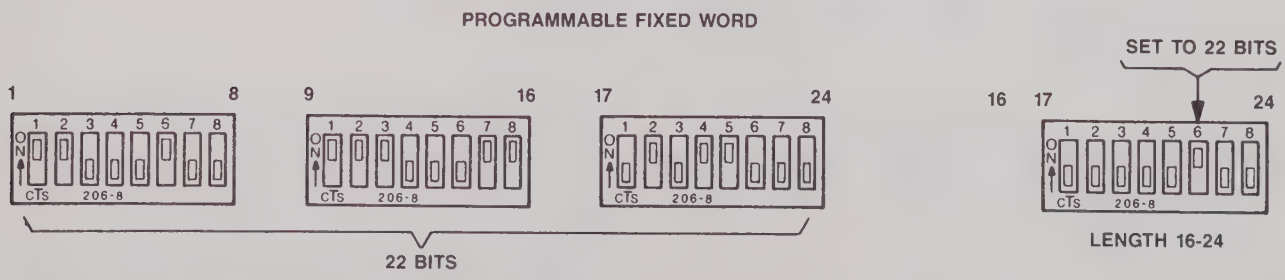


032185-11A

Toggle switch. Sets the S5104 Transmitter and Receiver for either **BIPOLAR** or **B8ZS** coding when the S5104 is set for the DS1 level. This setting affects both the S5104 Receiver and Transmitter.



EXAMPLE OF A 16-BIT WORD (NOTE: THE LENGTH 16-24 DIP SWITCHES ALL READ OFF). THE SEQUENCE (WORD) IS READ AS 1010111001101110.

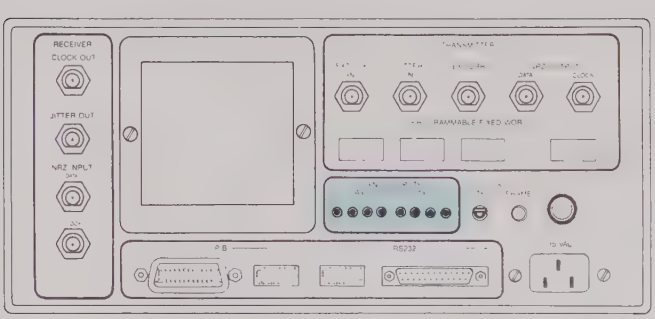


EXAMPLE OF A 22-BIT WORD. THE SEQUENCE IS READ AS 1100010011100011010110.

T-240784F

Fig. 12 – Programmable Fixed Word Setting Examples

2.4 SYNC OUTPUTS TEST POINTS



032185-11A

Four Receiver (**RX**) test points, three Transmitter (**TX**) test points, and a ground (**GND**). Test points are .040 inches (.10 cm) in diameter. Used to monitor M sync, PR sync, Bit Error sync, and BPV sync. The logic polarity is pulse high on all sync output test points. Test points are TTL compatible and are capable of driving 75 ohms and 10 feet (3 meters) of cable.

RX

Receiver Sync Output test points:

M — Occurs once per Master Frame in DS1C/DS2-level signals. M is synchronized with the first M-bit in a DS1C or DS2 Master Frame.

PR — Pseudorandom Repeat, which is coincident with the start of the PRBS. It is recognized by the occurrence of 19 zeros before zero suppression. Occurs once per $20^{20}-1$ pseudorandom sequence. (Pulse width is one-half the clock period.)

ERR — Bit error output or frame error in the LIVE mode. (Pulse width is one-half the clock period.)

BPV — Bipolar violation output. (Pulse width is one-half the clock output.)

TX

Transmitter Sync Output test points:

M — Occurs once per Master Frame in DS1C/DS2-level signals.

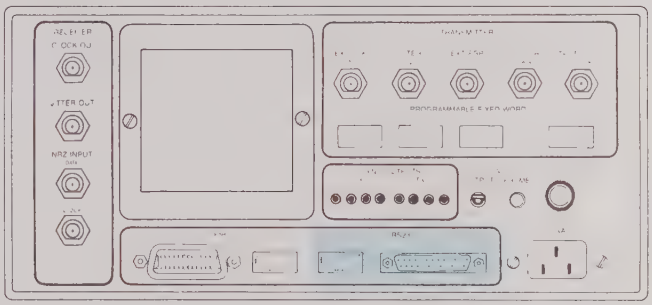
PR — Pseudorandom Repeat, which is coincident with the start of the PRBS. It is recognized by the occurrence of 19 zeros before zero suppression. Occurs once per $2^{20}-1$ pseudorandom sequence. (Pulse width is one-half the clock period.)

ERR — Pulse-synched to error insertion location. (Pulse width is one-half the clock period.)

GND

Ground for use with Transmitter and Receiver SYNC test points.

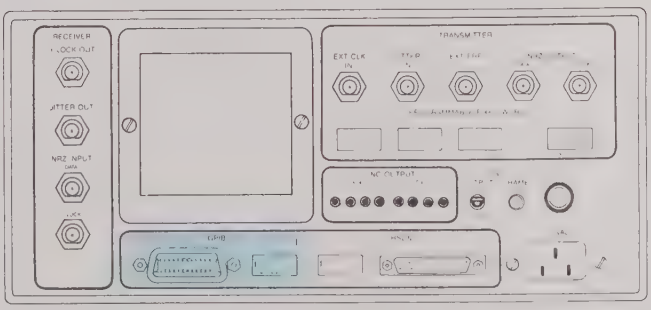
2.5 RS-232C INTERFACE



032185-11A

RS-232C Interface connector and DIP switches. Used for interfacing with peripheral equipment, data recording, and remote control. For complete and detailed information, refer to **SECTION 6, RS-232C INTERFACE.**

2.6 GPIB INTERFACE



032185-11A

IEEE-488 General Purpose Interface Bus connector and address DIP switches. Communicates as a talker/listener. For complete and detailed information, refer to **SECTION 5, GPIB (IEEE-488) INTERFACE.**

SECTION 3
WORKING WITH A PRINTER

3.1 THE ADVANTAGES OF USING A PRINTER WITH YOUR S5104

The S5104 is a powerful tool for digital performance testing. However, after you perform more than two tests or if you turn off the S5104, your test data is lost. By attaching a printer to your S5104, you can produce a permanent record of test results. S5104 test report printouts, which log the time and date of events, allow you to compare test results, diagnose problems, and distinguish trends.

3.2 SETTING UP A PRINTER

There is a standard two-way serial RS-232C Interface connector on the rear panel of your S5104. Any printer equipped with an RS-232C serial interface can be adapted for use with your S5104. However, we recommend Tau-tron's 5902 Printer which is designed for use with Tau-tron test sets. Refer to **SECTION 6, RS-232C INTERFACE** for the necessary pinout information and DIP switch setting to interface your printer with your S5104.

Tau-tron's 5902 Printer

Tau-tron's 5902 Printer is the ideal printer to use with your S5104. You can mount the printer on top of the S5104 with Tau-tron's "Stac-Trac" Mounting Kit as shown in Figure 13.

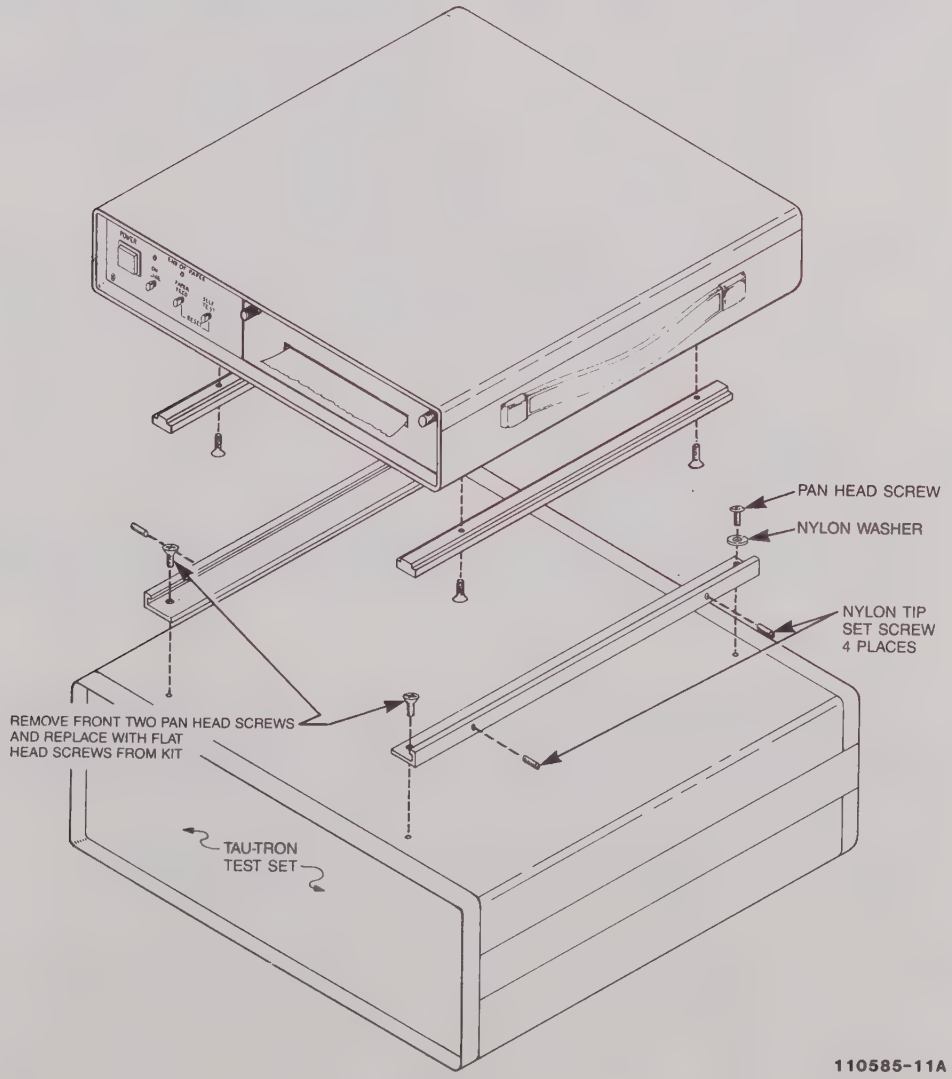

PAN HEAD SCREW
NYLON WASHER
NYLON TIP SET SCREW 4 PLACES
REMOVE FRONT TWO PAN HEAD SCREWS AND REPLACE WITH FLAT HEAD SCREWS FROM KIT
TAU-TRON TEST SET
110585-11A

Fig. 13 - Stac-Trac Mounting

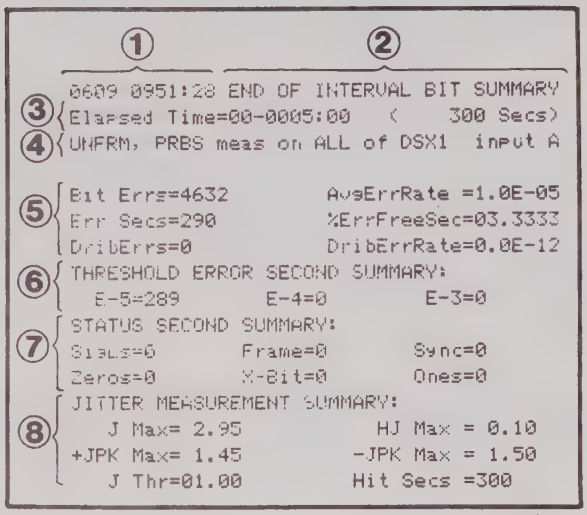
3.3 UNDERSTANDING SUMMARY REPORT PRINTOUTS

Summary reports are comprehensive printouts of test results. Before you attempt to print out a report, press the S5104 front-panel **AUX** pushbutton and select the desired type of report. A description and explanation of all reports follows.

3.3.1 End-of-Interval Summary Reports

One of the following three types of end-of-interval summary reports is printed at the end of a timed test: bit, frame, or BPV, depending on the type of measurement you select for printout. Figure 14 shows an example of an **END OF INTERVAL BIT SUMMARY.** Frame and BPV end-of interval summary reports have similar formats. However, Frame end-of-interval summary reports do not display Dribbling Error data or Threshold Errored Seconds.

Table A explains the meaning of the Summary Report printout data shown in Figure 14.


① ②
0609 0951:28 END OF INTERVAL BIT SUMMARY
③ Elapsed Time=00-0005:00 (300 Secs)
④ UNFRM, PRBS meas on ALL of DSX1 input A
⑤ Bit Errs=4632 AvgErrRate =1.0E-05
Err Secs=290 %ErrFreeSec=03.3333
DribErrs=0 DribErrRate=0.0E-12
⑥ THRESHOLD ERROR SECOND SUMMARY:
E-5=289 E-4=0 E-3=0
⑦ STATUS SECOND SUMMARY:
Slips=0 Frame=0 Sync=0
Zeros=0 X-Bit=0 Ones=0
⑧ JITTER MEASUREMENT SUMMARY:
J Max= 2.95 HJ Max = 0.10
+JPK Max= 1.45 -JPK Max = 1.50
J Thr=01.00 Hit Secs =300

022786-11A

Fig. 14 - End-of-Interval Summary Report

TABLE A
SUMMARY REPORT DEFINITIONS

NO.	DEFINITION
1	Date and time test was completed.
2	Type of Summary Report.
3	Total elapsed time of test prior to printout.
4	S5104 measurement settings. Includes: frame format (**FRM** or **UNFRM**), bit pattern (**PRBS**, **FIXED**, **ALL 1's**, or **THRU**), channel (**CH 1 - CH 4**), DS level (**DSX1 - DSX2**), and the input jack used to input the signal under test.
5	Error and error-rate data. • **Bit Errs** - Total number of errors (Bit, BPV, or Frame) that occurred during the test. • **Err Secs** - Total number of seconds in the test in which there were errors. • **DribErrs** - Total number of dribbling errors that occurred during the test. • **AvgErrRate** - Average error rate for the test expressed in scientific notation. For example, 1.0E-05 represents an average error rate of 1.0×10^{-5} or one error in every 100,000 bits. • **%ErrFreeSec** - Percentage of seconds that were free of errors during the test. • **DribErrRate** - Average dribbling-error rate for the test expressed in scientific notation.

TABLE A (CON'T)
SUMMARY REPORT DEFINITIONS

NO.	DEFINITION
6	Number of seconds in the test in which the error rate exceeded 1×10^{-5}, 1×10^{-4}, and 1×10^{-3} (E–5, E–4, and E–3).
7	Number of seconds in which the following status events occurred: • **SigLs** – Loss of signal • **Frame** – Loss of framing • **Sync** – Loss of pattern sync • **Zeros** – Detection of excess zeros • **X–Bit** – Detection of X–Bits • **Ones** – Detection of excess ones
8	Jitter measurement results. Note that either High-Frequency jitter or Jitter Threshold and Hit Second data is shown depending on which was selected for measurement. ***NOTE: If the Jitter Rx lost lock during the test, the results are squelched and the message "Jitter Rx lost lock" is printed.*** • **J Max** – Maximum peak-to-peak jitter amplitude, measured in Unit Intervals. • **HJ Max** – Maximum High-Frequency jitter amplitude measured during the test. • **+JPK Max** – Maximum +peak jitter measured during the test. • **–JPK Max** – Maximum –peak jitter measured during the test. • **J** or **HJ THR** – Either Jitter (**J**) or High-Frequency Jitter (**HJ**) peak-to-peak amplitude threshold setting. The threshold setting determines the amount of amplitude required to record a **J** or **HJ** Hit Second. • **Hit Secs** – Number of seconds during the test in which the **J** or **HJ** peak-to-peak jitter amplitude equals or exceeds the **J** or **HJ THR** setting.

3.3.2 Immediate Summary Reports

You can print an Immediate Summary Report at any time during an untimed or timed test. Immediate summary reports are printed in the same format as end-of-interval summary reports and show test results up to the time the report was printed.

To print an Immediate Summary Report, press the front-panel **AUX** pushbutton and enter **SNAPSHOT?**. Figure 15 shows an Immediate Summary Report.

```
0609 0944:56        IMMEDIATE BIT SUMMARY
Elapsed Time=00-0001:28   (     88 Secs)
UNFRM, PRBS meas on ALL of DSX1  input A

Bit Errs=1363          AvgErrRate =1.0E-05
Err Secs=85            %ErrFreeSec=03.4091
DribErrs=0             DribErrRate=0.0E-12
THRESHOLD ERROR SECOND SUMMARY:
  E-5=85         E-4=0          E-3=0
STATUS SECOND SUMMARY:
SigLs=0        Frame=0        Sync=0
Zeros=0        X-Bit=0        Ones=0
JITTER MEASUREMENT SUMMARY:
   J Max= 2.95              HJ Max = 0.10
+JPK Max= 1.45             -JPK Max = 1.50
   J Thr=01.00             Hit Secs =89
```

030386-11A

Fig. 15 – Immediate Summary Report

3.3.3 Power Loss Summary Reports

If the S5104 is set to print summary reports and power is lost, a Power Loss Summary Report is printed upon return of power. This occurs only if power input to the S5104 is interrupted and not if power is turned off with the front-panel **POWER** pushbutton.

The format of power loss summary reports is similar to end-of-interval and immediate summary reports. The time that power is regained is printed at the end of the report as shown in Figure 16.

```
0609 0953:36       POWER LOSS BIT SUMMARY
Elapsed Time=00-0001:10   (     70 Secs)
UNFRM, PRBS meas on ALL of DSX1  input A

Bit Errs=1090          AvgErrRate =1.0E-05
Err Secs=68            %ErrFreeSec=02.8571
DribErrs=0             DribErrRate=0.0E-12
THRESHOLD ERROR SECOND SUMMARY:
  E-5=68         E-4=0          E-3=0
STATUS SECOND SUMMARY:
SigLs=0        Frame=0        Sync=0
Zeros=0        X-Bit=0        Ones=0
JITTER MEASUREMENT SUMMARY:
   J Max= 2.95              HJ Max = 0.10
+JPK Max= 1.45             -JPK Max = 1.50
   J Thr=01.00             Hit Secs =71



0609 0953:40  RECOVERY FROM POWER LOSS
```

030386-11B

Fig. 16 – Power Loss Summary Report

3.3.4 Errored-Second Printouts

Your S5104 is able to print error information concerning any seconds in which errors occur during a test. To use this capability, press **AUX** and set **ERRSEC** to **ON**. An errored-second printout is printed for each second in which one or more errors occur. Figure 17 shows an errored-second printout, and Table B explains the meaning of the information contained in the report.

```
      (1)          (2)          (3)
0609 0957:32 Bit=16       J= 2.88
0609 0957:33 Bit=16       J= 2.90   (4)
0609 0957:34 Bit=2        J= 2.90
0609 0958:17 Bit=771869   J= 2.88    D
0609 0958:18 Bit=770813   J= 2.90    D
0609 0958:21 Bit=16       J= 2.88
0609 0958:23 Bit=1584896  J=Inval   D0
0609 0958:26 Bit=16       J=Inval
0609 0958:27 Bit=16       J=Inval
0609 0958:28 Bit=639828   J=Inval  Sg0
0609 0958:29 Bit=729482   J=Inval  Sg
0609 0958:30 Bit=654561   J=Inval  Sg
0609 0959:28 Bit=212508   J=Inval  FD
0609 0959:29 Bit=212832   J= 2.88 FD
0609 0959:30 Bit=212370   J= 2.88 FD
```

030386-11C

Fig. 17 – Errored-Second Printout

TABLE B
ERRORED-SECOND PRINTOUT DATA

NO.	DEFINITION
1	Date and time errored second occurred.
2	Total number of errors during the errored second.
3	Jitter or High-Frequency Jitter peak-to-peak jitter amplitude.
4	Status-second information. Mnemonics represent the following information: • **F** – Loss of frame • **D** – Loss of data bit synchronization • **Sg** – Loss of signal • **0** – Detect excess zeros • **1** – Detect excess ones • **X** – Detect X-Bits.

3.3.5 Squelching Errored-Second Printouts

During periods of high error rates, an errored-second printout can be printed every second. For tests of any significant duration, remember to check your supply of printer paper. You can set the S5104 to stop (squelch) printing errored-second printouts after ten consecutive errored seconds in which the error rate exceeds the errored-second squelch threshold. To set errored-second printout squelching, press **AUX** and set **SQUELCH** to the desired setting. Figure 18 shows an example of errored-second printout squelching.

```
0609 1002:23 Bit=155       J= 2.88
0609 1002:24 Bit=155       J= 2.88
0609 1002:25 Bit=155       J= 2.90
0609 1002:26 Bit=155       J= 2.90
0609 1002:27  ERR-SEC PRINTOUT SQUELCHED
0609 1002:43  ERR-SEC PRINTOUT REENABLED
0609 1002:58 Bit=155       J= 2.88
0609 1002:59 Bit=155       J= 2.90
0609 1003:00 Bit=155       J= 2.90
0609 1003:01 Bit=155       J= 2.88
0609 1003:02 Bit=155       J= 2.90
0609 1003:03 Bit=155       J= 2.90
0609 1003:04 Bit=155       J= 2.90
0609 1003:05 Bit=109       J= 2.90
```

030386-11D

Fig. 18 – Errored-Second Printout Squelching

SECTION 4
S5104 APPLICATIONS

This section describes specific applications for your S5104. The following subjects are discussed:

- Looptiming the S5104
- Generating CSU Loopback Codes Using the S5104.

4.1 LOOP TIMING THE S5104

During the course of testing a digital system, occasionally the need arises to frequency-lock the DS1, DS1C, or DS2 digital signal, generated by the S5104 Transmitter, with another DS signal that is currently being processed. This is especially true with digital switches where all inputs must be of exactly the same frequency. Under normal conditions, the S5104 Transmitter uses its own internal crystal clock source which is independent of any external sources; therefore, it is unlikely that the S5104 would be synchronized with any other signals.

To frequency-lock, or looptime the S5104 to another source, use the **RECEIVER CLOCK OUT** and **TRANSMITTER EXT CLK IN** jacks on the S5104 rear panel (see Figure 19) according to the following method:

First, a decision must be made as to which **DS** signal will be used to frequency-lock the S5104. Set up the S5104 Receiver for operation at the matching DS rate. At a convenient monitoring point, connect the S5104 Receiver to this reference signal. If this signal is a framed signal, any of the three receiver input **PATTERN** selections can be used in the **FRAME** mode. If it is unframed, either the **PRBS** or **FIXED PATTERN** in the **UNFRAME** mode can be used. It is normal for the S5104 not to have synchronization if the pattern selected does not match the pattern of the reference DS signal. This does not affect clock recovery. The setup configuration is identical to the standard method used to check live traffic in a working system. Next, connect a BNC-to-BNC jumper between the **RECEIVER CLOCK OUT** and **TRANSMITTER EXT CLK IN** jacks on the rear panel of the S5104. The S5104 Transmitter should be set up for normal testing using the correct DS rate. The S5104 Transmitter is now frequency-locked to the live DS signal connected to the S5104 Receiver.

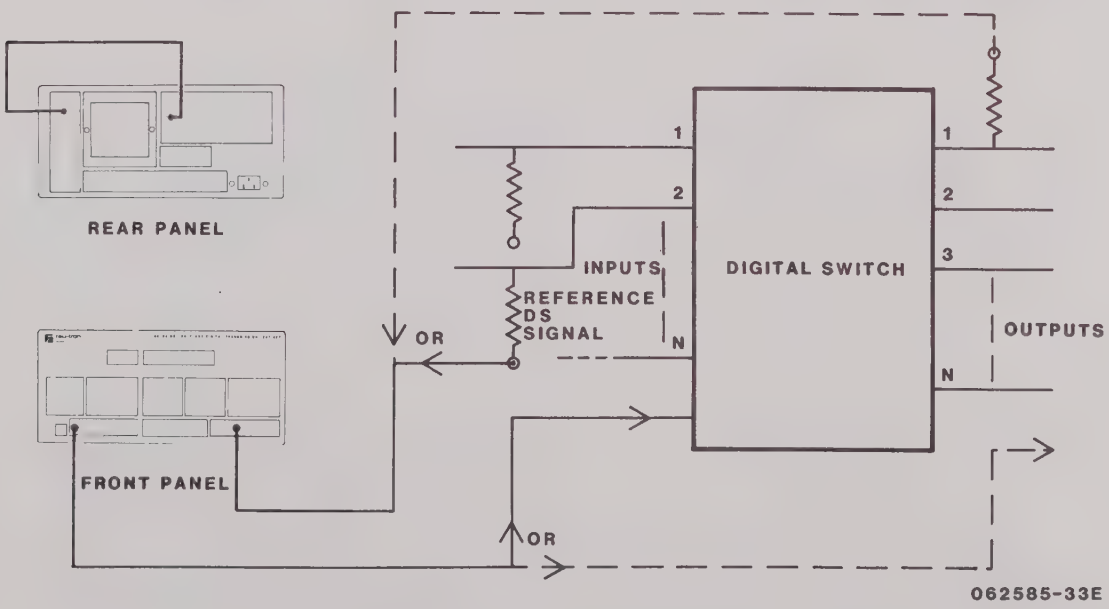


Fig. 19 – Loop Timing the S5104

One of the standard functions of the S5104 Receiver is to recover the clock signal from the incoming DS signal; in this case, the reference signal. This recovered clock is made available at the rear-panel **RECEIVER CLOCK OUT** jack. By using the jumper cable, you are connecting this clock source into the S5104 Transmitter, using it as the clock source to time the Transmitter. The S5104 Transmitter has a built-in activity detector to automatically determine when an external clock is being fed to it. No manual changeover is necessary to utilize the external clock input. The DS data generated by the S5104 is locked to the external clock input, which is derived from the reference DS signal.

This method of looptiming the S5104 can be used whenever the S5104 Transmitter must be frequency-locked to an existing signal.

4.2 GENERATING CSU LOOPBACK CODES USING THE S5104

AT&T Communications is planning to implement a new format for the DS1 rate. This new format is known as the Extended Superframe Format (ESF), also referred to as Fe. One of the implementation requirements is that the Digital Termination Equipment (DTE), sometimes called a Customer Service Unit (CSU), be able to loop itself back using either remote in-band or local commands. A block diagram of a Line Loopback (LLB) is shown in Figure 20.

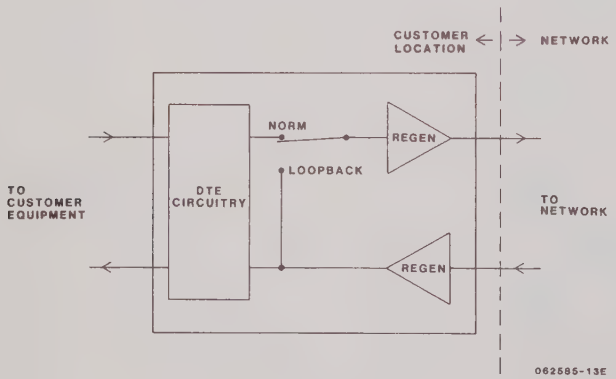


Fig. 20 – DTE Line Loopback

The Line Loopback configuration provides the network with a means to test the DS1 circuit, on an out-of-service basis, and in addition provides the capability to perform single-ended fault location of the digital line. When the DTE enters its loopback mode (Figure 20), it does not remove data errors or bipolar errors.

The DTE equipment can be commanded to activate or deactivate the LLB mode by either a full-rate DS1 in-band signal or a maintenance message implemented within the ESF format. Only the full-rate DS1 in-band implementation is addressed in this application.

The DTE enters the loopback mode whenever it recognizes a full-rate DS1 signal from the network consisting of a repeating pattern of one in five (00001), lasting for at least five seconds. The DTE returns to its normal operating mode when it recognizes a repeating pattern of one in three (001), lasting for at least five seconds. The DS1 signal can be either framed or unframed and still work correctly since the activation and deactivation patterns can have arbitrary values every 193rd bit position, overwriting the pattern.

If a method of generating the required codes is available along with a digital transmission test set, then line and transmission checkout would be possible without the need to gain physical access to the DTE for looping back. Considering the above requirements, Tau-tron's S5104 is the ideal digital transmission test set to perform the line and transmission tests and is also capable of generating the required loopback codes. This combination is extremely cost-effective and convenient, allowing a single test set to do both the testing and the loopback control.

The setup procedure is as follows:

The basic test setup and front-panel settings are shown in Figure 21. The **UNFRAME** setting will also work where other equipment in the system under test permits. At the Central Office or facility feeding the DS1 service to the customer, the facility transmission equipment is disconnected and replaced by the S5104. Normally, to perform a loopback test would require someone to physically effect a loopback at the customer location. Since physical access to the DTE may not always be possible, the test may not be able to be performed without the remote loopback capability.

Direct access to the DTE is no longer necessary and testing can proceed since the DTE can be remotely commanded to automatically effect the loopback connections. Simply set up the S5104 **PROGRAMMABLE FIXED WORD** to send the one in five code required to effect the loopback. Referring to Figure 22, set the word content switches, Numbers **5**, **10**, **15**, and **20** up. Set the length switch **20** up also. On the front panel, set the Transmitter to **DSX1**, **FIXED**, and either **FRAMED** or **UNFRAMED.**

After at least 5 seconds, the DTE should have internally looped back. The looped-back condition is indicated by the

S5104 gaining synchronization, providing the S5104 Receiver has been set, like the Transmitter, to **DSX1**, **FIXED**, and **FRAMED** or **UNFRAMED**. Figure 20 indicates what happens when the DTE internal switch goes to the loopback position. At this point, the **PRBS** or other programmable fixed-word pattern can be selected and testing can be started.

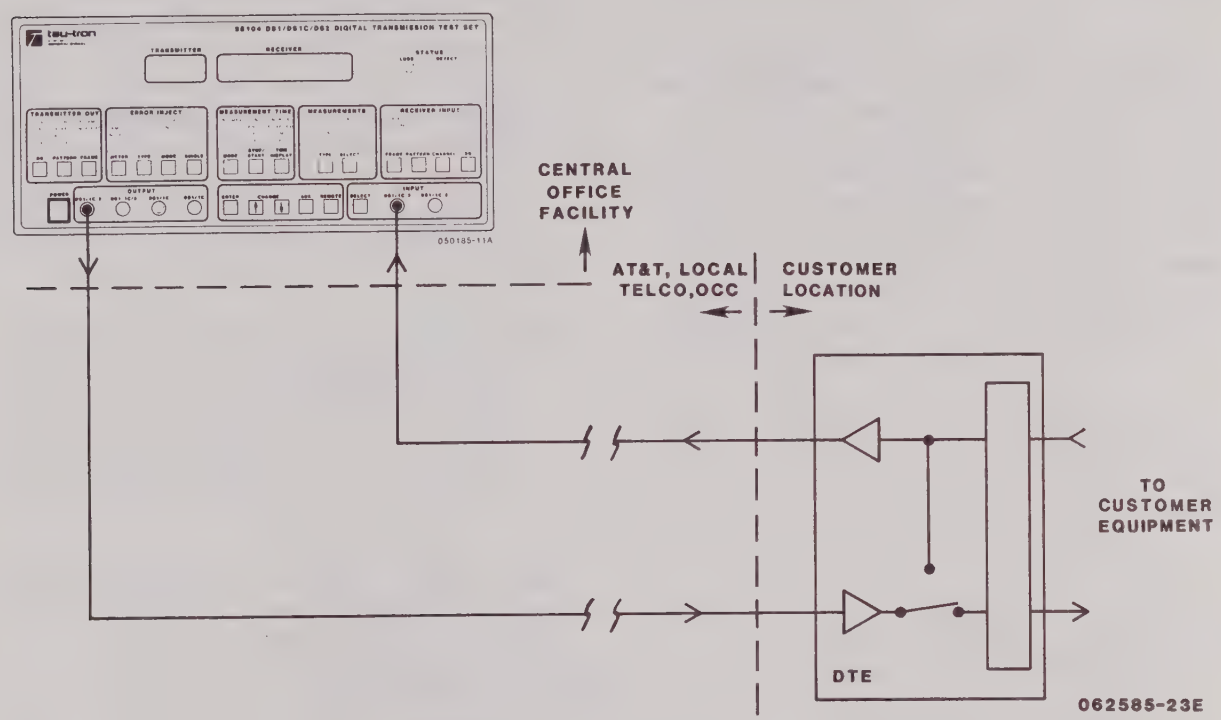


Fig. 21 – Line/Transmission Test Configuration

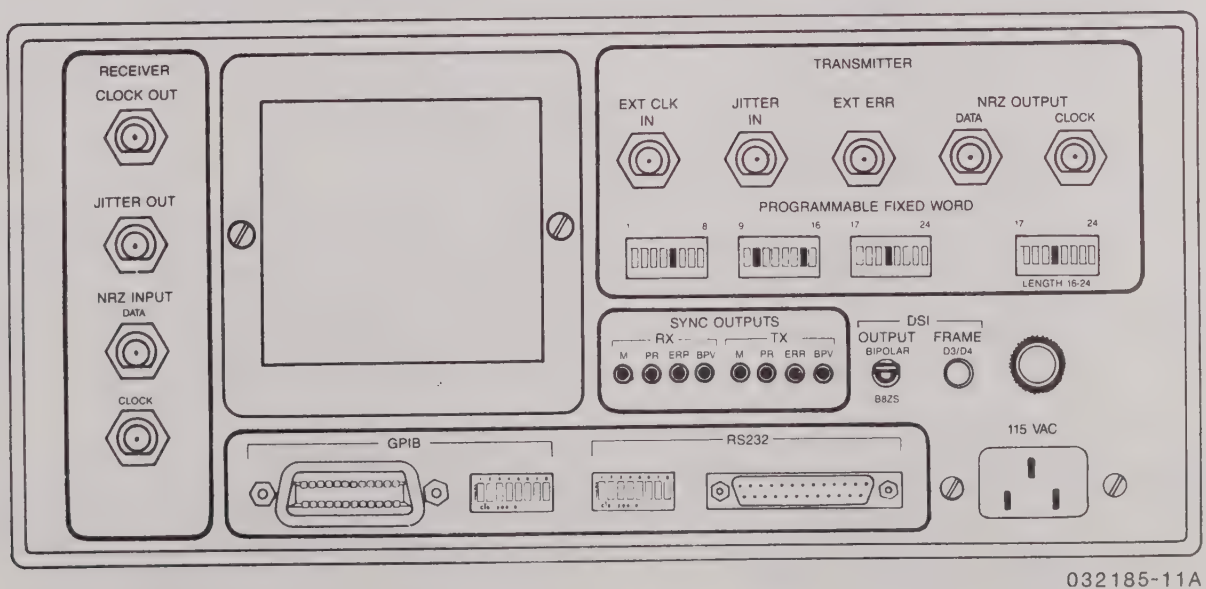


Fig. 22 – Activation Code

At the end of the testing, the loopback should be cancelled and the DTE returned to normal operation. This is done in a similar manner by setting up a fixed word consisting of a one-in-three code. This is shown in Figure 23. **PROGRAMMABLE FIXED WORD** content switches, Numbers **3**, **6**, **9**, **12**, **15**, and **18** are up; length switch **18** is also up.

The setup of Figure 21 is again employed. Normal operation of the DTE is indicated by the S5104 immediately gaining synchronization and then losing it after approximately five seconds. A signal appears to be present all the time, even when there is no customer equipment connected to the DTE and the DTE is no longer looped back, because the DTE emits a keep-alive all 1's signal when it has no input from the customer-provided equipment. The synchronization loss occurs because the transmitted code pattern is no longer looped back within the DTE; therefore, the pattern is no longer being recognized by the S5104 Receiver.

Any test patterns may be employed during testing except the two command codes described earlier. Also, the above procedures assume that: (1) the transmission medium between the DTE and S5104 is in good enough condition to accurately transmit the activation codes for the required minimum 5 seconds and that (2) the DTE code recognition and loopback circuitry is operating properly.

Further information on this topic is covered in AT&T Data Communications Technical Reference PUB 54016.

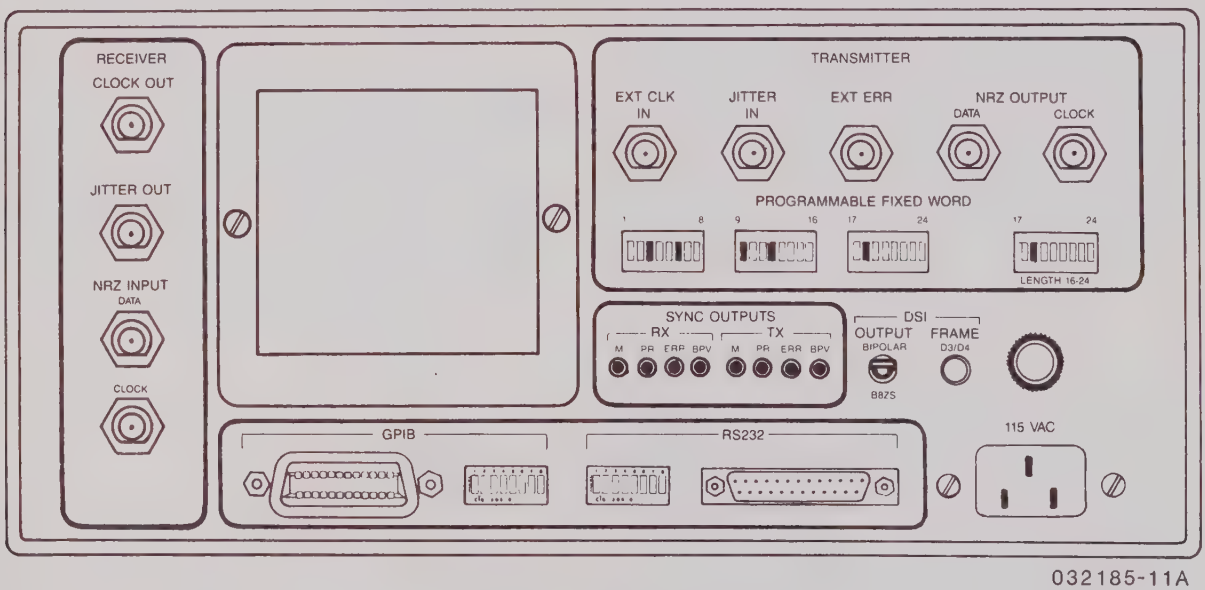


Fig. 23 – Deactivation Code

SECTION 5
GPIB (IEEE-488) INTERFACE

The S5104 can communicate with other GPIB-compatible devices as a talker/listener. This Section provides an introduction to the GPIB and details the S5104 GPIB capabilities.

5.1 IEEE-488 DESCRIPTION

The GPIB (General Purpose Interface Bus) transfers data and commands on a parallel-type bus structure. The interface functions for each instrument on the bus are performed within the unit. Therefore, only passive cabling is necessary to connect the system. The cables connect all instruments, controllers, and other units of the system in parallel across the signal lines.

Eight of the lines (DI01 through DI08) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous and coordinated by the three handshake lines: DAV (Data Valid), NRFD (Not Ready for Data), and NDAC (Not Data Accepted). The other five lines are for control of bus activity.

Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the roll of each of the other units by setting the ATN (Attention) line true and sending talk or listen addresses on the data lines (DI01 through DI08). Addresses are set into each device at the time of system configuration either by switches built into the unit or by jumpers on a printed circuit board. While the ATN line is true, all units must listen to the data lines. When the ATN line is false, only devices that have been addressed actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously, but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers should be unaddressed automatically.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as units can respond, but no faster than allowed by the slowest device being addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of five control lines. When ATN is true, ASCII-coded addresses and universal commands are transmitted on only seven of the data lines. When ATN is false, any code of eight bits or less understood by both the talker and listener(s) can be used.

The other control lines are IFC, REN, SRQ, and EOI. IFC (Interfacce Clear) places the interface system in an inactive state. REN (Remote Enable) is used with other coded messages to select either local or remote control of each unit.

Any active unit can set the SRQ (Service Request) line to true. This indicates to the controller that some unit on the bus wants attention; for example, a counter on a bus may want attention because it just completed a time-interval measurement and wants to transmit the reading to a printer.

EOI (End Or Identify) is used by a unit to indicate the end of a multiple-byte transfer sequence. When a controller sets both ATN and EOI lines to true, each unit capable of a parallel poll indicates its current status on the data line assigned to it (DI01 through DI08).

It is not necessary that every unit be capable of responding to all of the lines. Each unit can be designed to respond only to those lines that are pertinent to its functions on the bus.

5.2 S5104 TX/RX GPIB CAPABILITIES

The S5104 may be interfaced as a talker/listener or a talker only. No controller functions are implemented. As described in the IEEE-488 (GPIB) standard, the following GPIB capabilities are implemented:

- SH1 Complete source handshake
- AH1 Complete accepter handshake
- T5 Basic talker, serial poll, talk only, unaddress if addressed to listen
- TEO No extended talker (secondary talk address) capability
- L4 Basic listener, no listen only, unaddress if addressed to talk
- LEO No extended listener (secondary listen address) capability
- SR1 Complete service request capability
- RL1 Complete remote/local capability including local lockout
- PPO No parallel poll capability

- DC1 Complete device clear capability
- DT1 Complete device trigger capability
- CO No control capability
- E2 Tri-state drivers are used on DI0 lines to achieve maximum data transfer rates.

5.3 GPIB INTERFACE CONNECTIONS

A 24-pin **GPIB** connector is provided on the rear panel of the S5104. Connector dimensions and pinouts correspond to IEEE specifications. Tri-state drivers are used on the DI0 lines in the talk mode to achieve higher data transfer rates.

5.4 GPIB ADDRESS AND OPTION SELECTION

The 8-section DIP switch on the rear panel is used for GPIB talk/listen address and option selection, which follows in Table C and Figure 24.

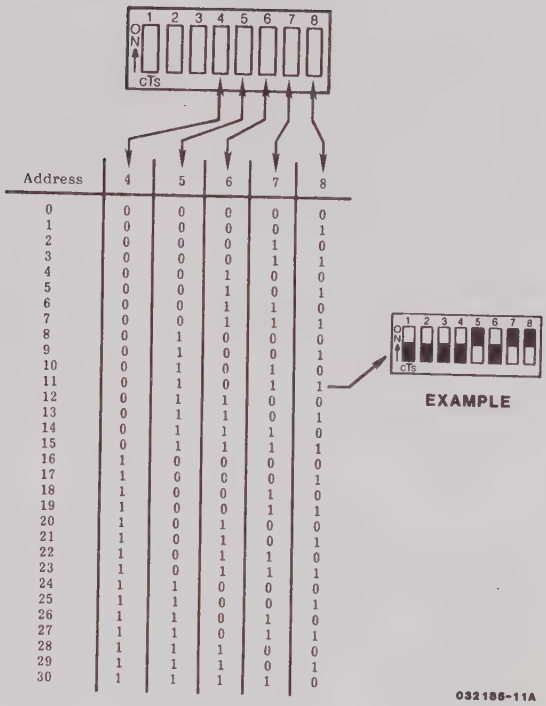


Fig. 24 – GPIB Address DIP Switch Setting

TABLE C
GPIB TALK/LISTEN ADDRESS DIP SWITCH SETTINGS

SWITCH	FUNCTION (1=ON=UP)	DESCRIPTION
1 (left)	SRQ Enable	With this switch on, the S5104 is allowed to generate service requests (assert the GPIB SRQ line). In systems with many GPIB units, this may not be desirable. Service requests can be inhibited by setting this switch down to its off position. The S5104 maintains status and responds to serial polls regardless of the SRQ Enable setting.
2	Talk Only	With this switch on, the S5104 may be used in a system with a listen-only printer and no controller. In this mode, print functions can be selected from the front panel and the printer output sent to a GPIB printer. The S5104 ignores all GPIB commands when in a talk-only mode (switch 2 up). Switch 2 should be down (off) for normal talker/listener operation.
3	Listen Only	This setting is ignored by the S5104 since it does not have a listen-only mode of operation.
4 5 6 7 8	Address A5 Address A4 Address A3 Address A2 Address A1	A1 through A5 plus two additional bits, independent of the switch settings, form a 7-bit talk and listen address. A1 is the least-significant bit, A2 is the next most significant, etc. The two additional bits are the most-significant bits and are fixed as 1–0 for a talk address, and as 0–1 for a listen address. Once the five address bits A1 through A5 are selected, both talk and listen addresses are specified for the S5104.

NOTE: The DIP Switch is read on power-up only. To change the S5104 GPIB address or other characteristics, the S5104 must be turned off, then turned back on again.

Several GPIB capabilities are not supported by the S5104 test set. The following commands are ignored by the S5104:

- Identify (parallel poll trigger)
- Secondary addresses
- Parallel poll configure/unconfigure
- Parallel poll enable/disable
- Take control

The following paragraphs detail the GPIB commands and events to which the S5104 responds.

5.5 RESPONSE TO GPIB COMMANDS

The S5104 responds to the following GPIB commands and events:

- Addressed to listen
- Universal unlisten command
- Addressed to talk
- Universal untalk command
- Data byte received
- Interface clear command
- Remote/local command
- Local lockout command
- Device clear command
- Device trigger command
- Serial poll enable/disable command

S5104 Test Set Addressed to Listen

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
MLA	Y 0 1 L L L L L 5 4 3 2 1	1 x x x x
L1 – L5 specify the device-dependent bits of the device's listen address as set by the rear-panel DIP switch.		

When MLA (My Listen Address) is present on the GPIB bus, the S5104 is addressed to listen. If previously addressed to talk, the S5104 automatically untalks. The S5104 cannot be configured to talk and listen at the same time to prevent its talk data from being interpreted as commands.

Universal Unlisten Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
UNL	Y 0 1 1 1 1 1 1 1	1 x x x x

When UNL (Unlisten) is present on the GPIB bus, the S5104 ceases to listen and addressed commands (GET, GTL, and SDC) and data are ignored. Universal commands (IFC, REN, DCL, SPE, SPD, MLA, and MTA) continue to be responded to and recognized.

S5104 Test Set Addressed to Talk

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
MTA	Y 1 0 T T T T T 5 4 3 2 1	1 x x x x
T1 – T5 on the DIO lines specify the device dependent bits of the device's talk address as set by the rear-panel DIP switch.		

When MTA (My Talk Address) is present on the GPIB bus, the S5104 is addressed to talk. If previously addressed to listen, the S5104 automatically unlistens to prevent output data from being interpreted as commands. Since a GPIB system can have only one talker, unique talk addresses must be selected for each device in the system. All other devices must untalk when the S5104 is addressed to talk. If addressed to talk after SPE (Serial Poll Enable) and before SPD (Serial Poll Disable), the S5104 responds by putting its status byte on the DI0 lines (described later under **SERVICE REQUEST AND SERIAL POLL RESPONSE**). Otherwise, S5104 output data (i.e., measurements) are placed on the DI0 lines. If the S5104 has nothing to say, it outputs one or two null bytes along with the EOI signal.

Universal Untalk Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
UNT	Y 1 0 1 1 1 1 1	1 x x x x
OTA	OTA = SGA ∧ MTA	
The UNT code is provided for system use.		

The presence of UNT (Untalk) command or a talk address other than OTA (Other Talk Address) causes the S5104 to become unaddressed to talk. If service requests are not inhibited and the S5104 still has data it wishes to output, a service request indicating request-to-talk is generated.

Data Byte Received

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
ATN	x x x x x x x x	1 x x x x
DAB	D D D D D D D D 8 7 6 5 4 3 2 1	0 x x x x
D1 – D8 specify the device dependent data bits. The source of the message on the ATN line is always the C function, whereas the messages on the DIO and EIO lines are enabled by the T function.		

When the GPIB ATN (Attention) line is inactive and the S5104 is addressed to listen, bytes received on the eight DI0 lines are interpreted as device-dependent commands.

Interface Clear Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
IFC	x x x x x x x x	x x x 1 x

When the IFC (Interface Clear) line is asserted on the GPIB bus, the S5104 reinitializes its interface functions as described by IEEE-488-1978 state diagrams. A pending service request is cleared. The status byte in the S5104 is not cleared, however. It may be polled to determine if bus errors, indicated in the status byte, may have caused bus problems prior to the interface clear command. If previously in remote mode, IFC does not return the test set to local control.

Remote/Local Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
GTL	Y 0 0 0 0 0 0 1	1 x x x x
LLO	Y 0 0 1 0 0 0 1	1 x x x x
REN	x x x x x x x x	x x x x 1

When the REN (Remote Enable) line is asserted on the bus and the S5104 is addressed to listen, the test set is placed in remote mode and the front-panel **REMOTE** indicator is illuminated. While in remote mode, all local control (front-panel pushbuttons) is disabled except the return-to-local key (REMOTE). If the LLO (Local Lockout) command is issued, the front panel return-to-local key is also disabled.

The S5104 may be placed under remote control only by first asserting the REN line and then being addressed to listen. When in remote mode, REN going inactive returns the unit to local control. If the S5104 is addressed to listen in remote, the presence of the GTL (Go to Local) message returns the S5104 to local control.

Device Clear Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
DCL	Y 0 0 1 0 1 0 0	1 x x x x
SDC	Y 0 0 0 0 1 0 0	1 x x x x

The S5104 may be cleared by DCL (Universal Device Clear) or SDC (Selective Device Clear). SDC is accepted by the S5104 only if it has been addressed to listen. DCL is responded to in any mode. In response to a device clear command, the test set re-executes its power-up initialization sequence, including reinitializing its GPIB interface function. If previously addressed to talk or listen, the S5104 returns to its unaddressed state.

NOTE: At least a few seconds should be allowed before issuing any further commands to give the S5104 time to complete its power-up reinitialization sequence.

This command provides a simple way to return the S5104 to a known state, the power-up state.

Device Trigger Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
GET	Y 0 0 0 1 0 0 0	1 x x x x

When GET (Group Execute Trigger) command is present on the GPIB bus and the S5104 has been addressed to listen, it executes its stop/start function. This action is identical to stopping or starting receiver measurements using the **STOP START** pushbutton.

Serial Poll Enable/Disable Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
SPD	Y 0 0 1 1 0 0 1	1 x x x x
SPE	Y 0 0 1 1 0 0 0	1 x x x x

The SPE (Serial Poll Enable) and SPD (Serial Poll Disable) commands are recognized by the S5104 when they are present on the bus. In response to a serial poll, the S5104 puts its GPIB status byte on the DI0 lines. The serial poll command sequence and status byte interpretation are described later under Service Request and Serial Poll.

5.6 DEVICE-DEPENDENT COMMANDS

All S5104 capabilities controllable from the front panel may be remotely controlled. A set of device-dependent commands issued on the GPIB selects S5104 commands. When the S5104 is addressed to listen, data accepted on the DI0 lines are interpreted as test set commands.

Programming the S5104 in remote control is as simple as programming it by front-panel entry. Commands correspond to front-panel pushbutton selects. These commands must be issued in the same sequence as front-panel pushbuttons to select test set functions. Additional commands are provided to return test set status or **SNAPSHOT** the TX and RX displays. Device-dependent commands are summarized in Table D.

5.6.1 Command Sequence Formats

All device-dependent command sequences must be issued in the following format:

Command 1 (delimiter, command 2)
(delimiter, command 3) . . . . CR

Commands are read as 7–bit ASCII codes off the DI0 lines. Multiple commands in a command sequence must be delimited by any of the following valid delimiters. Every command sequence must be terminated by a Carriage Return (CR).

DELIMITER		ASCII CODE (HEX)
SP	(blank)	20
NULL	(null byte)	00
,	(comma)	2C
;	(semicolon)	3B
HT	(tab)	09

5.6.2 Command Errors

Valid commands may be treated as invalid if they have no meaning in the S5104's current mode. For example, when editing transmitter internal error rate, only the Enter (ENT), Increment (INC), Decrement (DEC), and Transmitter Error Mode (XMO) commands have meaning. Unrecognized commands or commands invalid due to context cause the command error bit to be set in the S5104's serial poll status word. If service requests are enabled, command errors also generate a service request.

Table D provides a list of S5104 remote-control commands. All S5104 Transmitter and Receiver functions can be remotely controlled, and all status returned to the remote controller with these commands. Control commands duplicate front-panel key functions. Setup status commands return the current state of the S5104. Additional status and display **SNAPSHOT** commands may be used to access displayed measurements and signal status. Commands are arranged in three groups: 1) Transmitter commands, 2) Receiver commands, and 3) Common commands.

TABLE D
REMOTE CONTROL COMMANDS

FUNCTION	CONTROL COMMAND	PUSH-BUTTON	STATUS COMMAND	INDICATOR STATE	ASCII STATUS
TX Format & Level	XDS	DS	XDS?	DSX1 DSX1C DS2H DSX2	0 1 2 3
TX Pattern	XPA	PATTERN	XPA?	PRBS FIXED ALL 1's THRU	0 1 2 3
TX Frame	XFR	FRAME	XFR?	FRAMED UNFRAMED	0 1
TX Error Type	XTY	TYPE	XTY?	BIT BPV	0
TX Error Mode	XMO	MODE	XMO?	ERR FREE INT INT EXT	0 1 (Edit) 3 (Inject) 2
Single Error Inject	XSI	SINGLE	None	None	None
TX Jitter Inject	XJI	JITTER	XJI?	DISABLE INT EXT	0 1 2
TX Jitter Display	XJD	JITTER	XJD?	FREQ AMPL INT EXT	0 1 2 3
Snapshot TX Display	XDP	None	XDP?	ERROR JITTER	0 **(Note 1)** 1
RX Format & Level	RDS	DS	RDS?	DSX1 DSX1C DS2H DSX2	0 1 2 3
RX Channel	RCH	CHANNEL	RCH?	CH 1 CH 2 CH 3 CH 4	0 1 2 3
RX Pattern	RPA	PATTERN	RPA?	PRBS FIXED LIVE	0 1 2
RX Frame	RFR	FRAME	RFR?	FRAMED UNFRAMED	0 1

TABLE D (CON'T)
REMOTE CONTROL COMMANDS

FUNCTION	CONTROL COMMAND	PUSH-BUTTON	STATUS COMMAND	INDICATOR STATE	ASCII STATUS
RX A/B Input Selection	RIN	SELECT	RIN?	Left/A Right/B	0 1
RX Measurement Type	RTY	TYPE	RTY?	BIT BPV FRAME STATUS JITTER	0 1 2 3 4
RX Measurement Select	RSE	SELECT	RSE?	None	**(Note 2)**
RX Time Mode	RMO	MODE	RMO?	UNTIMED SINGLE REPEAT	0 1 2
Stop/Start Test	RST	STOP/ START	RST?	IN PROC STOP/SET	0 1
Time Display	RTI	TIME DISPLAY	RTI?	INTRVAL ELAPSED TIME DATE	0 1 2 3
Snapshot Signal Status	None	None	RCS?	STATUS	**(Note 3)**
Snapshot History Status	None	None	RHS?	STATUS	**(Note 3)**
Snapshot RX Display **(Note 4)**	RDP	None	RDP?	MEASURE TIME AUX	0 1 2
Enter	ENT	ENTER	None	None	None
Change Increment	INC	CHANGE ↑	None	None	None
Change Decrement	DEC	CHANGE ↓	None	None	None
Auxiliary Functions	AUX	AUX	None	None	None
Return-to-Local Control	RTL	REMOTE	RTL?	REMOTE Local	1 0
Initialize to Power-Up State	DCL	None	None	None	None
Go to Remote Mode	REM	None	RTL?	REMOTE Local	1 0
Lockout Return-to-Local	LLO	None	LLO?	Locked Unlocked	1 0
Unlock Local Lockout	LLU	None	LLO?	Locked Unlocked	1 0

TABLE D (CON'T)
REMOTE CONTROL COMMANDS

NOTE 1: The command **XDP** *"snapshots" the current Transmitter display and outputs the four- to six-character ASCII result to the remote interfaces. Display formats are summarized in the following:*

DISPLAY TYPE	FORMAT
Error Injection Displays:	
Error Free	'____'
Internal Error Rate/Rate Set	'nE-x'
External Error Rate	'n.n-x'
Jitter Injection Displays:	
Internal Generated Jitter Frequency	'n.nn,x'
Internal Generated/External Applied Amplitude	'nn.nn'
Internal/External Jitter Disabled	' OFF'
Internal/External Jitter Enabled	' ON'

NOTE 2: The ASCII status code returned in response to the **RSE?** *command depends on the current measurement-type selected for display (***BIT, BPV, FRAME, STATUS,** *or* **JITTER)***. If measurements are not currently being displayed, this command returns the status code of the last displayed measurement (i.e., the measurement which would be displayed the next time measurements are selected). The following list provides ASCII status by measurement type:*

MEASUREMENT	STATUS
BIT and BPV Measurements:	
Total Errors Since Start of Test	0
Current Error Rate Over 10**7 Bits	1
Average Error Rate Since Start of Test	2
Total Errored Seconds Since Start of Test	3
E-5 Threshold Errored Seconds Since Start of Test	4
E-4 Threshold Errored Seconds Since Start of Test	5
E-3 Threshold Errored Seconds Since Start of Test	6
Total Dribbling Errors Since Start of Test	7
% Error Free Seconds Since Start of Test	8
Frame Error Measurements:	
Total Frame Errors Since Start of Test	0
Average Error Rate	1
Total Frame Errored Seconds	2
% Frame Error-Free Seconds Since Start of Test	3
Status Second Measurements:	
Signal Loss Seconds	0
Frame Loss Seconds	1
Data Sync Loss Seconds	2
Excess Zeros Seconds	3
All Ones Detected Seconds	4
X-Bit Detected Seconds	5
Jitter Measurements:	
Current Jitter Amplitude	0
Maximum Jitter Amplitude Since Test Start	1
Current High-Frequency Jitter Amplitude	2
Maximum High-Frequency Jitter Amplitude Since Start of Test	3
Jitter Threshold	4
Jitter Threshold Hit Seconds	5

TABLE D (CON'T)
REMOTE CONTROL COMMANDS

NOTE 3: Signal status (either current or history) is reported back as a 7-digit ASCII representation of the binary state of each status indicator. When current status is requested **(RCS?)**, *0's indicate that the corresponding status is not currently active; 1's indicate that the associated status condition is currently detected. When history status is requested* **(RHS?)**, *0's indicate that the corresponding status has not been detected since the start of test; 1's indicate that status was or is detected. The 6-digit word is formatted as* **SFDZOXL** *where:*

S = 1 if Signal loss detected; 0 if not.
F = 1 if Frame loss detected; 0 if not.
D = 1 if Data sync loss detected; 0 if not.
Z = 1 if Excess Zeros detected; 0 if not.
O = 1 if All Ones detected; 0 if not.
X = 1 if X-bit detected; 0 if not.
L = 1 if Jitter lost lock; 0 if not (Jitter RX).

NOTE 4: The **RDP** *command "snapshots" the current Receiver display and outputs the 10-11 character ASCII result to the remote interfaces. The following illustrates display formats:*

DISPLAY FUNCTION	FORMAT
Measurements:	
Error Measurements:	
Total Errors Since Test Start	'nnnnnnn TOT'
Current Error Rate Over 10**7 Bits	'n.nE-x BER'
Average Error Rate Since Test Start	'n.nE-xx AVG'
Total Errored Seconds Since Test Start	'nnnnnn ESEC'
E-5 Threshold Errored Seconds Since Test Start	'nnnnnn E-5'
E-4 Threshold Errored Seconds Since Test Start	'nnnnnn E-4'
E-3 Threshold Errored Seconds Since Test Start	'nnnnnn E-3'
Total Dribbling Errors Since Test Start	'nnnnnnn DRB'
% Error-Free Seconds Since Test Start	'nn.nnnn %EF'
Status Second Measurements:	
Signal Loss Seconds	'nnnnnn SGLS'
Frame Loss Seconds	'nnnnnn FRAM'
Data Sync Loss Seconds	'nnnnnn SYNC'
Excess Zeros Seconds	'nnnnnn ZERO'
All Ones Detected Seconds	'nnnnnn ONES'
X-Bit Detected Seconds	'nnnnnn XBIT'
Jitter Measurements:	
Current Jitter Amplitude	'nn.nn JCUR'
Maximum Jitter Amplitude Since Test Start	'nn.nn JMAX'
Current +Peak Amplitude	'nn.nn J+PKCU'
Maximum +Peak Amplitude	'nn.nn J+PKMX'
Current −Peak Amplitude	'nn.nn JPKCU'
Maximum −Peak Amplitude	'nn.nn J−PKMX'
Current High-Frequency Jitter	'nn.nn HJCUR'
Maximum High-Frequency Jitter Since Test Start	'nn.nn HJMAX'
Jitter Threshold (Amplitude)	'nn.nn J_THR'
Jitter Threshold (High-Frequency)	'nn.nn HJ_THR'
Jitter Threshold Amplitude Hit Seconds	'nnnnnn JHS'
Jitter High-Frequency Jitter Hit Seconds	'nnnnnn HJHS'

TABLE D (CON'T)
REMOTE CONTROL COMMANDS

DISPLAY FUNCTION		FORMAT
Time:	Time Interval	' dd-hhmm:ss'
	Elapsed Time	' dd-hhmm:ss'
	Time-of-Day	' hhmm:ss'
	Date	' dd-mmm-yy'
Auxiliary Functions:		
Printer:		
	Printer Function Select Prompt	'PRINTER? '
	Printer Off/Bit/BPV Select	'PRINT xxx'
	Errored-second Printout Off/On Select	'ERRSEC xxx'
	Errored-second Printout Squelch Select:	
	No Squelching (All Err Secs Printed)	'SQELCH OFF'
	Squelch On E-5/E-4/E-3 Error Rate	'SQU ON E-x'
	Squelch On Any Errors	'SQU ON ANY'
	Snapshot Measurements for Summary and/or Recall	'SNAPSHOT?'
	Recall Measurement Display Off/On	'RECALL xxx'

In general, control commands are of the form FAA where F is an X or an R for Transmitter or Receive function, respectively, and AA is the first two characters of the associated key's front-panel label. For example, XFR is the command for the Transmitter key labeled **FRAME**. Exceptions occur when this convention would create duplicate commands (there are two RX SELECT keys). Status commands are formed by simply adding a '?' to the end of the corresponding control command; i.e., XFR? returns current transmitter framing mode.

5.7 S5104 OUTPUT TO GPIB

As shown in Table D, the S5104 provides commands to access every front-panel control. Status information can also be returned as needed. In addition, several other commands are provided to **SNAPSHOT** Transmitter and Receiver displays and Receiver signal status (current and history). These commands and the corresponding output format are included in Table D.

5.7.1 Status Output Commands

All S5104 status outputs are formatted as ASCII messages terminated by a carriage return. If multiple status command are sent in a single command line, each output message is separated by a carriage return. For example, the command sequence RFR?, RPA? would result in 0 <CR> 0 <CR> being queued for output if the current receiver framing and pattern were **FRAMED** and **PRBS**.

5.7.2 Display Output Commands

Two commands, XDP and RDP, are provided to **SNAPSHOT** the current Transmitter and Receiver displays, respectively. After receipt of one of these commands, the S5104 outputs the ASCII-formatted display message when addressed to talk. The message is terminated by a carriage return. Since all S5104 measurements can be displayed on the Receiver display, all measurement capabilities are available or output to a remote controller.

Displays are described in detail in preceding sections covering Transmitter and Receiver front-panel opertion. Table D shows the format for all display functions.

5.7.3 Automatic Print Functions

Errored-second and summary measurements may be obtained by selecting test set printer outputs and configuring the instrument to talk. These outputs are particularly useful when the test set is in the talk-only mode, outputting to a listen-only printer.

5.8 SERVICE REQUEST AND SERIAL POLL RESPONSE

Several conditions detected in the S5104 cause it to request service of the GPIB controller. The ability of the S5104 to request service may be inhibited by the rear-panel DIP switch.

When the controller detects a service request, it should serial poll the S5104 to determine if it is requesting service and why. In response to a Serial Poll addressed to the S5104, the S5104 places its 8-bit GPIB status byte on the DI0 lines. The S5104 clears its status byte when it receives a Serial Poll Disable

(SPD) command. The GPIB status byte is also cleared on power-up in response to device clear. Only the service request bit in the status byte is reset by an interface clear.

5.8.1 Service Request, GPIB Status Byte

The following conditions cause the S5104 to request service if SRQ is enabled:

- Bus Error (BIT 1) – A bus error occurs when the S5104 is addressed to talk with no listeners active on the bus. Since a source handshake may have been started by the talking S5104 with no acceptor to complete the handshake, this error may hang-up the bus. This condition can be cleared and detected by the controller issuing an interface clear followed by a serial poll. The ON condition for the bit is 1.

- Cmd Error (BIT 2) – A command error occurs when the S5104 detects an invalid device-dependent command as described earlier under **DEVICE-DEPENDENT COMMANDS**. The command error bit is set in the GPIB status byte. The ON condition for the bit is 1.

- Talk Request (BIT 0) – When the S5104 has data to output but is not addressed to talk, it generates a service request with the talk request bit set in the GPIB status byte. The ON condition for the bit is 1. If configured to talk before serial polled, this bit is cleared in the status byte. If no other bits are set, the service request is de-asserted.

- Power Loss (BIT 3) – If power to the S5104 is lost and recovered, the POWER LOSS bit is set in the GPIB status byte. Commands issued while power was lost are not accepted by the S5104. On recovery from power failure, the S5104 may not be in the mode commanded by the controller. The ON condition for the bit is 1.

The SRQ bit is ON (1) whenever one or more of the other bits (power loss, cmd error, bus error, or talk request) are ON and service request has been enabled by DIP switch 1.

Multiple bits may be set in the status byte when it is polled. All bits are cleared following a serial poll.

Status displayed by front-panel indicators is not available through the GPIB status byte acquired by serial polling. S5104 status may be obtained as described earlier under Output Status Commands.

The S5104 does not respond to parallel polling commands.

5.8.2 Serial Polling

The GPIB status byte may be accessed from the S5104 by serial polling as follows:

1. Issue 'UNT' universal untalk command.
2. Issue 'SPE' serial poll enable command.
3. Issue controller listen address.
4. Issue 'MTA' at the S5104 talk address.
5. Receive 'STB' at the S5104 status byte.
6. Issue 'UNT' or 'OTA' S5104 test set untalk command.
7. Issue 'SPD' serial poll disable command.

NOTE: A random loss of the SRQ bit may occur after the S5104 has generated a service request and has been polled. The user should check for any bits set in the serial poll status word to determine if the S5104 may have requested service.

SECTION 6
RS-232C INTERFACE

The RS-232C Interface provides the S5104 with a standard two-way serial interface. The interface may be used to output measurements to a printer or to any other device with an RS-232C Interface. It may also be used to remotely control and access data from the S5104 using a terminal or computer.

This appendix describes the RS-232C Interface, the serial data format, and how to connect the S5104 to RS-232C devices.

6.1 INTERFACE CONNECTIONS

A 25–pin D-connector labeled **RS-232** is provided on the rear panel of the S5104 for use with external equipment. The signals that are used are wired in accordance with EIA RS-232C standards for Data Terminal Equipment (DTE).

PIN	NAME	FUNCTION
1	GND	Protective Ground.
2	TxD	Transmitted Data Output: Bit-serial data stream. Format is selected by rear-panel DIP switch.
3	RxD	Received Data Input: Bit-serial data stream. Commands to the S5104 are received on this input. Format selected by rear-panel DIP switch.
4	RTS	Request to Send Output: Hi-level when S5104 has data for output.
5	CTS	Clear to Send Input: Hi-level indicates external device, such as a printer, is ready to accept data. This line must be high to enable the S5104 to output data. A low-level indicates the output device is busy or its buffer is full.
6	DSR	Data Set Ready Input: Unused.
7	GND	Signal Ground.
8	DCD	Received Line Signal Detect Input: (Carrier detect) High-level (>3V) indicates an external device, such as CRT terminal, wants to send commands to the S5104. This line must be high to enable the S5104 to accept input commands on line 3. When this signal is absent or low, inputs on line 3 are ignored.
20	DTR	Data Terminal Ready Output: Set to on (>3V) by the S5104.
ALL OTHER PINS		No connection.

The S5104 may be configured for full-duplex or half-duplex operation. In full-duplex mode, all characters received without error on the received data line (pin 3) are echoed back to the source on the transmit data line. No echoing is done in half-duplex mode. During full-duplex operation, commands and data may be simultaneously received and transmitted. In half-duplex operation, only one function, transmit or receive, may take place at a time. The Request to Send (RTS), Clear to Send (CTS), and Data Carrier Detect (DCD) signals control which function is active on a half-duplex channel. The RS-232C standard defines when transitions on the RTS, CTS, DSR, DTR, and DCD lines may take place.

6.2 SERIAL DATA FORMAT

Data is output from the S5104 in an asynchronous bit-serial fashion at one of eight selectable baud rates. The format of the bit-serial data stream is shown in Figure 25.

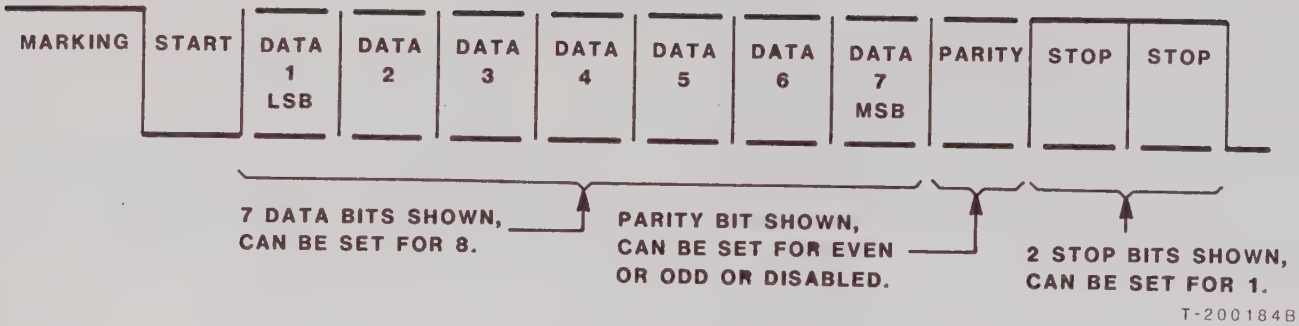


Fig. 25 – Bit-Serial Data Stream Format

6.3 BAUD RATE AND OPTION SELECTION

The data baud rate, number of bits per character, parity selection, and number of stop bits are selected by the rear-panel DIP switch. Switch assignments are as follows:

DIP SW	BAUD RATE	SW SEC. (1 = ON) 1	2	3
1 (L)	110	0	0	0
2	150	1	0	0
3	300	0	1	0
	600	1	1	0
	1200	0	0	1
	2400	1	0	1
	4800	0	1	1
	9600	1	1	1
4	Bits/Char	0=7, 1=8		
5	Parity Disable	0		
	Parity Enable	1		
6	Odd Parity	0		
	Even Parity	1		
7	1 Stop Bit	0		
	2 Stop Bits	1		
8 (R)	Half Duplex	0		
	Full Duplex	1		

NOTE: The DIP Switch is read on Power-Up only. To change the S5104's baud rate or other characteristics, the unit must be turned off, then turned back on.

6.4 S5104 REMOTE CONTROL COMMANDS

All S5104 capabilities controllable from the front panel may be controlled remotely. Programming the S5104 via the RS-232C Interface is as simple as programming it by the front-panel controls. Most commands correspond to front-panel pushbuttons. These commands must be issued in the same sequence as front-panel commands. Additional commands are provided to acquire measurements and status, or to reinitialize the S5104 to its power-up state.

6.4.1 Remote Command Sequences

All commands must be issued in the following format:

CMD 1 (delimiter CMD2) (delimiter CMD3) . . . CR

CMD 1, 2, 3, etc., are any of the commands shown in Table D in SECTION 5. Command mnemonics are read from the RS-232C receive data line (pin 3). Command sequences may contain one or more commands and must be terminated by a carriage return and line feed. A command sequence must not exceed 128 characters in length. Multiple commands in a command sequence must be separated by any of the following valid delimiters:

DELIMITER		ASCII CODE (HEX)
SP	(blank)	20
NULL	(null byte)	00
,	(comma)	2C
;	(semicolon)	3B
HT	(tab)	09

The S5104 backspaces and deletes received characters when the ASCII backspace (HEX 08) or rubout (HEX 7F) character is received. In full-duplex mode, the received backspace or rubout character is echoed to the remote controller. In addition, the unit echoes a carriage return and line feed when a carriage return is received. Commands are not accepted and responded to until the carriage return is received.

6.4.2 Response to Commands and Command Errors

When the carriage return terminating a command sequence is received, the S5104 decodes and responds to the command sequence. Multiple commands in a sequence are responded to one at a time. If any of the commands are improper, the S5104 outputs **WHAT?** to the RS-232C Interface, but responds to all valid commands in the sequence. If all commands in the sequence are valid, the S5104 outputs **OK** to the RS-232C Interface. **WHAT?** or **OK** is output in both full- and half-duplex modes. If the S5104 is in the middle of sending printer outputs or requested data, the command acknowledgments may be interspersed with the data.

Two types of errors may occur. If parity detection is enabled, each received character is checked for proper parity. Characters with improper parity are ignored. In full-duplex operation, only characters with the correct parity are echoed to the remote controller, indicating their acceptance.

Invalid commands are ignored by the S5104. If a multiple command sequence contains an invalid command, valid commands in the sequence are still interpreted and responded to. Since many S5104 remote commands depend on previous commands, sequences containing an invalid command may be misinterpreted. Valid command mnemonics may be treated as invalid commands if they have no meaning in the S5104's current mode. When editing transmitter error rate, only the ENTER (ENT), CHANGE (INC and DEC), and transmitter error MODE (XMO) commands have meaning. Any other command, such as transmitter PATTERN (XPA), is ignored and the S5104 responds with **WHAT?**.

6.5 INTERFACING TO OTHER RS-232C DEVICES

Interfacing the S5104 to another RS-232C device is simple if you know the pinout and configuration of the other device. All DTE devices transmit on line 2 and receive on line 3. All DCE devices transmit on line 3 and receive on line 2. Different printers typically provide their clear-to-send (printer ready for data) handshake on different lines. A null modem may be necessary to cross-connect the printer handshake to the S5104's clear-to-send input. The S5104 must see clear-to-send active before it transmits data. It continues to transmit data at the specified baud rate until the clear-to-send line goes inactive or there is no more data to be output. The S5104 must be set (by rear-panel DIP switches) to transmit at the same baud rate, parity selection, and data word length as the receiving device. Generally, the S5104 should be set to transmit 2 stop bits. This gives the receiving device a better chance to resynchronize on the next start bit.

The S5104 must see receive line signal detect (pin 8) active before it accepts data on its receive data line (pin 3). A modem provides this signal on pin 8 whenever it has detected a carrier (i.e., phone link completed to another modem). If the S5104 is connected directly to a terminal, it may be necessary to cross-connect the terminal's power-on signal (often pin 20, data terminal ready) to the S5104's pin 8 input.

6.5.1 Interfacing an RS-232C Terminal to the S5104

The RS-232C Interface specification allows many different configurations. Data rate, format, and content are not strictly specified. Therefore, getting a device's RS-232C Interface to talk to another device often requires some initial configuration.

Once familiar with RS-232C Interface standards, the following procedure simplifies interface setup.

STEP	PROCEDURE
1	Determine the terminal's (or printer, modem, computer, or other RS-232C device) RS-232C pinout. Consult user manual for terminal to determine its pinout. Make proper connection as previously described in this section. A null modem may be required to cross-connect transmit, receive, and handshake signals.
2	Determine terminal's serial data format. Set the S5104's format to match.
3	Turn on terminal and S5104. Using the **AUX** pushbutton, enable bit printouts, select **SNAPSHOT**, and verify output at terminal. If no output or garbled output occurs, use RS-232C INTERFACE TROUBLESHOOTING, which follows this procedure, as a guide to determine and correct the problem.
4	When the previous step is completed successfully, press the **RETURN** key on the terminal. Verify **OK** or **WHAT?** response output to the terminal. If no response, consult RS-232C INTERFACE TROUBLESHOOTING, which follows this procedure.
5	After successfully completing the last step, type in a sequence of commands corresponding to a valid sequence of key depressions. Verify that the S5104 responds to the commands and sends back an **OK** response.

6.6 RS-232C INTERFACE TROUBLESHOOTING

The EIA RS-232C Interface specification allows many different configurations. Data rates, format, and content are not strictly specified. Getting one device's RS-232C Interface to talk to another device often requires some initial configuration. Rear-panel DIP switches on the S5104 permit the user to configure the instrument's RS-232C Interface to match the characteristics of many RS-232C peripherals. This section lists problems commonly encountered when attempting to make the S5104 communicate via an RS-232C Interface, along with procedures to follow for their solutions.

The RS-232C specification defines separate transmit and receive data lines. The S5104 outputs bit-serial information over the transmit data line (pin 2 of the connector). Many printers, including Tau-tron's 40–Column Printer, expect data on the receive data line (pin 3). If this is the case, the S5104's transmit data line must be connected to the printer's receive data line.

For the S5104 to transmit data, its clear-to-send input (pin 5) must be active (>3V). The printer supplies this signal on its data-terminal ready line (pin 20). Again, the null modem makes the required cross-connection. If the printer is off-line or busy (not ready to accept data), it drives this line inactive, signaling to the S5104 to stop sending data to the printer.

The S5104 expects to receive remote commands in bit-serial form on its receive data line (pin 3). For the S5104 to accept commands on its receive data line, its received line-signal detect input (pin 8, sometimes called data carrier detect) must be active (>3V).

The serial data stream consists of a start bit, 7 or 8 data bits, possibly a parity bit, and 1 or 2 stop bits. The baud rate, number of data bits per character, and parity bit selection must match the format expected by the printer. The S5104 should generally transmit two stop bits, while the printer should look for one. The configuration of these interface characteristics is controlled by DIP switches on the rear panel of the S5104.

NOTE: DIP switches are read only on power-up. If a configuration change must be made, the S5104 must be turned off, the appropriate DIP switches set, and the S5104 turned back on.

When the rate at which printer output is generated exceeds the printer capability to store and print it, some data is lost. The RS-232C clear-to-send handshake line is enabled for the S5104 to output the data to the printer. When the printer is busy, off-line, or out of paper, it may disable this line, signaling the S5104 to discontinue output. As more error seconds occur, print messages continue to be generated in the S5104. Queue storage (1024 bytes) is provided for backing-up data. When this queue pace is filled, the S5104 keeps track of the number of buffers lost. Each print buffer corresponds to a 40–character print line. When the printer is again ready for data, the number of lost buffers is reported in hexadecimal form.

The source of nearly all interface problems is improper connections and/or mismatches in the transmitted and expected data rate or format. The following table lists several commonly encountered symptoms, likely causes, and solutions.

TABLE E
PRINTER/INTERFACE TROUBLESHOOTING

PROBLEM SYMPTOM	POSSIBLE CAUSE	SOLUTION
Printer fails to print any data	Printer off	Plug-in printer and turn printer on.
	Printer off-line	Some printers, including Tau-tron's 5902, have an on-line/OFF-LINE switch. Make sure the printer is on-line.
	Cable not connected	Connect RS-232C cable.
	Improper connection	Make sure pin 2 from S5104 is wired to printer's input data line. Make sure pin 5 input at S5104 is receiving clear-to-send indication from printer.

TABLE E (CON'T)
PRINTER/INTERFACE TROUBLESHOOTING

PROBLEM SYMPTOM	POSSIBLE CAUSE	SOLUTION
Printout is garbled	Data rate or format mismatch	Set the S5104 to off and set the rear-panel DIP switches to select proper baud rate, parity, and number of data bits/character to match printer setup. Set the S5104 to on.
Character occasionally lost in printout	Sync loss	Set the S5104 to off and rear-panel DIP switch for 2 stop bits. Set printer for 1 stop bit. Set the S5104 to on.
Multiple characters occasionally lost in printout	Data overrun	Printer is not toggling the S5104 clear-to-send line when it is busy and unable to accept data. S5104 keeps transmitting and data is lost. Provide signal from printer to pin 5 of S5104 interface. Signal must be active ($>3V$) when printer is ready to accept data and inactive ($<-3V$) when printer is busy.
S5104 outputs print functions to terminal but does not accept remote commands	Improper connection	Make sure the S5104 data line (pin 3) is connected to the remote controller's transmit data line. Make sure the S5104 receive line signal detect (pin 8) is active (connected to modem Carrier Detect or remote controller power-on or ready line).
	Data format mismatch	Set the S5104 to off and set rear-panel DIP switches to select parity and number of data bits per character to match remote-controller setup. Set the S5104 to on.
Characters typed at remote control terminal do not appear on screen, but are accepted by the S5104	Terminal in full duplex; S5104 in half duplex	Set the S5104 to off. Set the S5104 switch 8 to on. Set the S5104 to on; S5104 echoes all received characters to verify their reception.

SECTION 7
S5104 THEORY OF OPERATION

This section explains the theory of operation of the S5104 Digital Transmission Test Set.

The S5104 Digital Transmission Test Set consists of 11 plug-in printed circuit (PC) boards, a motherboard, a front-panel board, a rear-panel board, and a power-supply board (see Figure 26). The S5104 is powered by either 115 Vac or 230 Vac (factory-wired option).

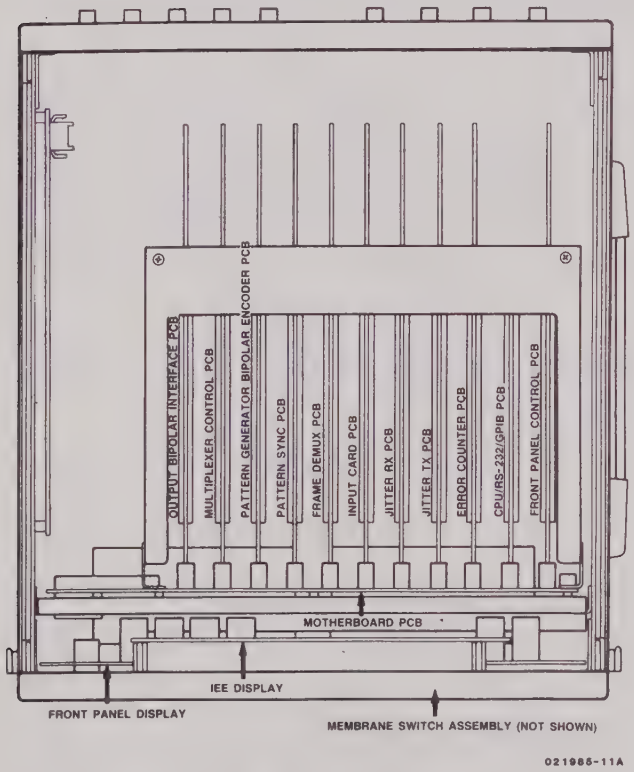


Fig. 26 – S5104 Plug-in PC Boards

7.1 SYSTEM CONCEPT

The S5104 system (see Figure 27) can be divided into three subsystems:

- Transmitter and Receiver control functions and data processed through the status and control bus
- Front-panel control pushbuttons, indicators, and displays and the Error Counter, Jitter TX, Jitter RX, and the CPU/RS-232C/GPIB PC boards which are processed through the standard bus
- Power distribution

The Front Panel Control PC board is the communication interface between the status and control bus and the standard bus.

7.2 STATUS AND CONTROL BUS

The transmitter section that uses the status and control bus consists of the Multiplexer Control PC board, the Pattern Generator Bipolar Encoder PC board, and the Output Bipolar Interface PC board.

7.2.1 Multiplexer Control PC Board

The Multiplexer Control PC board generates the data-stream signals. These are the DS1 (1.544 MHz), the DS1C (3.152 MHz), and the DS2 (6.312 MHz) level signals, referred to as internally generated clock signals. An external clock signal can be processed instead of the internal clock signals. The rear-panel **EXT CLK IN** BNC connector can accept a clock signal between 1 and 7 MHz, which is sent to the Multiplexer Control PC board to be processed. A detected external clock signal overrides internal clock signals.

Mark sync pulses are generated by the Multiplexer Control PC board and sent to the **M SYNC** test point on the rear panel.

Transmitter data and clock signals are sent to the Pattern Generator Bipolar Encoder PC board via the status and control bus.

7.2.2 Pattern Generator Bipolar Encoder PC Board

The Pattern Generator Bipolar Encoder PC board establishes the data pattern of the DS signals. The pseudorandom bit sequence (**PRBS**), **ALL 1's** (111. . .), and **FIXED** patterns are generated by this PC board. The **FIXED** pattern is set by the rear-panel **PROGRAMMABLE FIXED WORD** DIP switches.

The DS output pattern is generated by the Pattern Generator Bipolar Encoder PC board and selected by the rear-panel **DS1 OUTPUT** toggle switch. Either a **BIPOLAR** or a **B8ZS** (Bipolar 8-Zero Substitution) pattern can be selected. The B8ZS pattern format is generated by taking NRZ signals and sending them to a B8ZS encoder.

NRZ (Non-Return to Zero) data and clock signals are generated from the Pattern Generator Bipolar Encoder PC board and sent to the **NRZ OUTPUT DATA** and **CLOCK** BNC connectors on the rear panel.

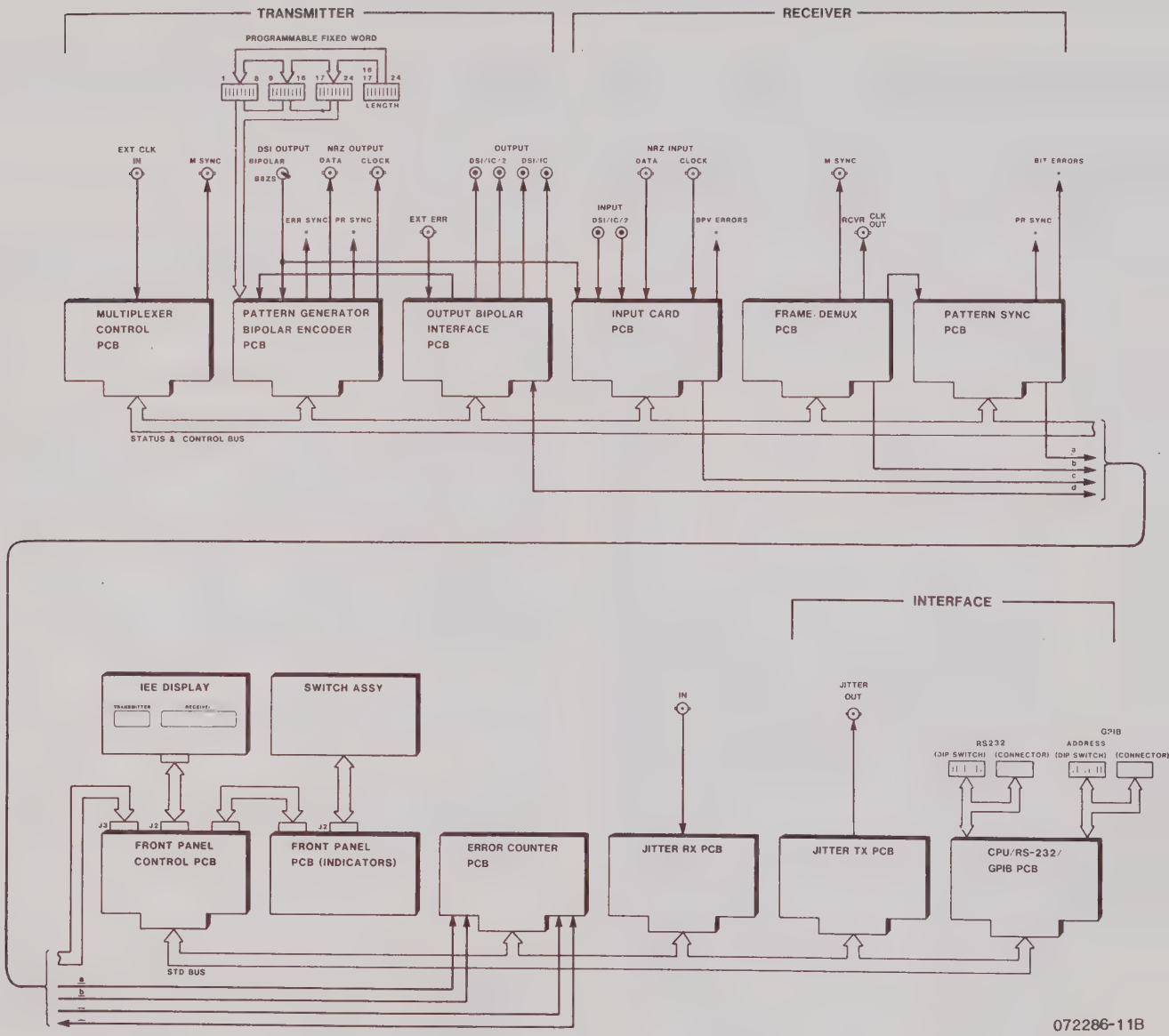


Fig. 27 – S5104 System Functional Block Diagram

Error sync pulses are generated and sent to the rear-panel **ERR SYNC** BNC connector. PR sync pulses are generated and sent, once every pseudorandom sequence (every $2^{20}-1$ bits), to the **PR SYNC** test point on the rear panel.

7.2.3 Output Bipolar Interface PC Board

The Output Bipolar Interface PC board accepts the DS1/1C/2 signals, amplifies them, and sends them to an output buffer. The signals are then output to two **DS1/1C/2** and two **DS1/1C OUTPUT** jacks on the front panel. These signals are the prime output test signals.

External errors, applied to the rear-panel **EXT ERR** BNC connector, are inserted on the Pattern Generator board and interfaced on the Output Bipolar Interface PC board. Clock-rate errors generated by this PC board are sent to the Error Counter PC board. All errors received at the Error Counter PC board produce a μs error signal that is sent to the Output Bipolar Interface PC board.

The receiver section that uses the status and control bus consists of the Input PC board, the Frame/Demux PC board, and the Pattern Sync PC board.

7.2.4 Input PC Board

The Input printed circuit board acts as the interface for receiver input signals. DS1, DS1C, or DS2 signals can be sent to the Input PC board from the two front-panel **INPUT DS1/DS1/1C/2** jacks. NRZ data and clock signals are received from the rear-panel **NRZ INPUT DATA** and **CLOCK** BNC connectors.

Errors from this board, such as BPV and signal loss, are sent to the Error Counter PC board. DS data and clock signals received by the Input PC board are sent to the Frame/Demux PC board.

7.2.5 Frame/Demux PC Board

Signals received by the Frame/Demux PC board are processed into patterned (framed) data and clock signals and then sent to the Input PC board and the Pattern Sync PC board. The Frame/Demux PC board finds frame and demultiplexes the signals.

Frame loss and X–bit errors are sent to the Error Counter PC board. Frame error is sent to the Pattern Sync PC board.

Mark sync pulses generated by the Frame/Demux PC board are sent to the rear-panel **RECEIVER M SYNC** test point.

7.2.6 Pattern Sync PC Board

The Pattern Sync PC board receives pattern data and clock signals and synchronizes the incoming signals while searching for errors. The pattern sync output is sent to the rear-panel **PR SYNC** test point.

Detected bit errors are sent to the rear-panel (bit) **ERR** test point. Sync loss is detected and sent to the Error Counter PC board.

7.3 STANDARD BUS

7.3.1 Error Counter PC Board

The Error Counter PC board receives all errors to be counted. The errors are received by accumulators on the board that count the errors and then send the count to a storage register. The storage register makes counts available to the Front-Panel Control PC board via the standard bus.

An error received by the Error Counter PC board produces a μs error signal that is sent to the Output Bipolar Interface PC board.

7.3.2 Jitter TX and RX PC Boards

The Jitter TX and RX PC boards are used to generate and receive jitter within the system. The Jitter TX PC board contains a jitter frequency generator which is controlled by an internal microprocessor.

The rear-panel **JITTER IN** and **JITTER OUT** BNC connectors allow for external jitter modulation and are used as a jitter output monitor.

7.3.3 CPU/RS-232/GPIB PC Board

The CPU/RS-232/GPIB PC board performs the central processing functions and the RS-232C and GPIB interfacing functions. This board contains the microprocessor system 4.9152-MHz oscillator (clock), the Z80 microprocessor, and the input/output bus interface circuitry.

A rear-panel **GPIB ADDRESS** DIP switch and an **RS-232** DIP switch are used to configure the GPIB and RS-232C interfaces.

7.3.4 Front-Panel Control PC Board

The Front-Panel Control PC board communicates between the PC boards on the status and control bus and the PC boards on the standard bus. Front-panel controls, indicators, and displays connect to the Front-Panel Control PC board to interact with the system. A 32.768-kHz signal is generated within this board for the time-of-day clock. A 3.6-Vdc rechargeable battery pack on this board maintains memory and clock data during power failures.

SECTION 8

PRINTED CIRCUIT BOARD CONFIGURATION SETTINGS

This section describes settings (jumper and DIP switch configurations) that can be made on internal PC boards. The S5104 arrives from the factory in a normal setting or configuration but may be changed as detailed in this section.

8.1 SYNCHRONOUS/ASYNCHRONOUS ERRORED SECONDS

An 8-section DIP switch on the CPU PC board (Figure 28) can be used to reconfigure the S5104 from the normal factory setting of synchronous errored seconds to asynchronous errored seconds. The switch numbered **1** is set **ON** for synchronous errored seconds or off for asynchronous errored seconds. This DIP switch is also used to configure other options. Table F lists the other DIP-switch settings.

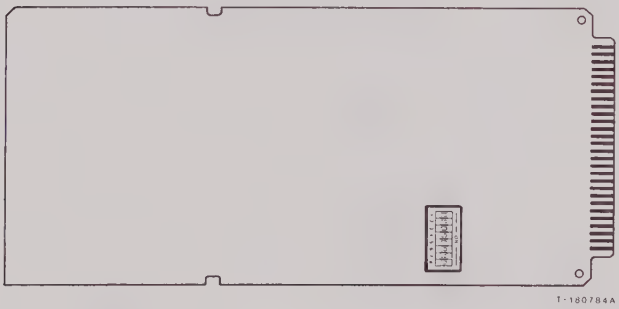


Fig. 28 - CPU PCB DIP Switch Location

8.2 CLOCK AND DATA PHASING

The clock edge, or phasing, of the Transmitter and Receiver clock and data signals can be switched 180°. This is accomplished by reconfiguring the jumpers on the Pattern Generator and/or the Input PC boards (Figure 26 shows the location of these PC boards).

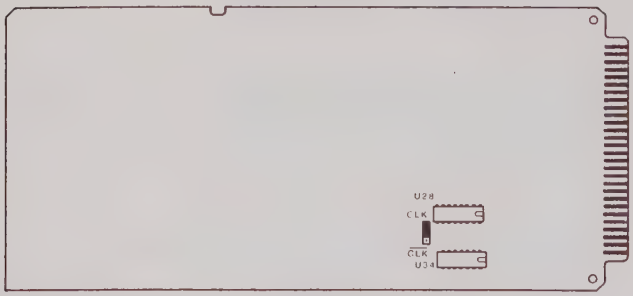
The Transmitter clock and data signals are sent out the rear-panel **NRZ OUTPUT DATA** and **CLOCK** BNC connectors. The signals are generated by the Pattern Generator PC board. A jumper on this PC board (Figure 29) allows the signals to be configured for **CLK** or $\overline{\textbf{CLK}}$. From the factory, the jumper is set over the two pins adjacent to the **CLK** position. **CLK** sets the rising edge of the output clock in the center of the data bit. Placing the jumper over the two pins adjacent to the $\overline{\textbf{CLK}}$ position sets the edge of the output clock in the center of the data bit.

The Receiver clock and data signals are received by the rear-panel **NRZ INPUT DATA** and **CLOCK** BNC connectors. The signals are sent to the Input PC board. A jumper on the Input PC board (Figure 30) allows the signals to be inverted (changed 180°). From the factory, the jumper is set over the two pins that do not invert the phasing of the signal (rising edge of input clock is in center of data bit). Positioning the jumper in the alternate position inverts the signals (falling edge of input signal is in the center of the data bit).

TABLE F

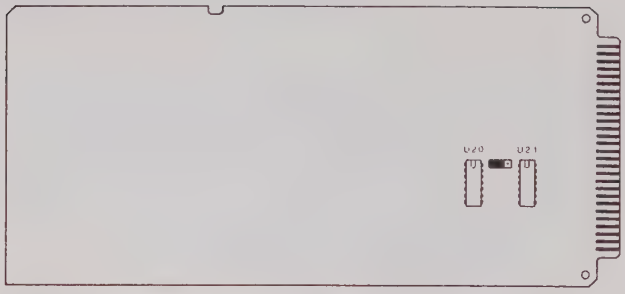
CPU/RS-232/GPIB PCB DIP-SWITCH SETTINGS

DIP SWITCH	DEFINITION
1	Off = Asynchronous ERR SECS On = Synchronous ERR SECS
2	Off = RS-232C not installed On = RS-232C installed
3	Off = Halt on failure On = Restart on failure
4	Off = Jitter option not installed On = Jitter option installed
5	Off = GPIB not installed On = GPIB installed
6	Off = CPU/RS-232C PCB installed On = CPU/GPIB/RS-232C PCB installed
7	Off = Jitter TX not installed On = Jitter TX installed
8	Not used



NOTE: BLACK INDICATED THE FACTORY SET JUMPER POSITION FOR Tx CLOCK. T-180784B

Fig. 29 – Pattern Generator PCB Jumper Location



NOTE: BLACK INDICATED THE FACTORY SET JUMPER POSITION FOR Rx CLOCK. T-180784C

Fig. 30 – Input PCB Jumper Location

SECTION 9
S5104 SPECIFICATIONS

9.1 TRANSMITTER SPECIFICATIONS

CLOCK (Internal)	
Frequency:	
DS1	1.544 MHz ± 15 ppm
DS1C	3.152 MHz ± 15 ppm
DS2	6.312 MHz ± 15 ppm
Stability	±10 ppm at 32° to 122°F (0° to 50°C), ±3 ppm aging rate per year
CLOCK (External)	
Frequency	1 MHz to 7.0 MHz
Impedance	75 ohms
Level	Amplitude of 2.5 to 5V. Baseline of 0 volts.
Interface	Rear panel BNC connector
Selection	Automatically selected when external frequency is connected to the rear panel BNC connector.
OUTPUT (Bipolar)	
Code:	
DS1	AMI or B8ZS (Selectable by rear-panel switch)
DS1C	AMI
DS2	B6ZS
Level:	
DS1	±3.0V ±0.3V
DS1C	±3.0V ±0.3V
DS2H1	±2.1V ±0.25V
DSX2	High output in series with 1,000 ft (300m) ABAM cable simulator
Pulse Shape	Compatible with CB119
Impedance	110 ohms, balanced
OUTPUT (Binary)	
Data/Clock Level	2.5V to 5.0V amplitude logic 1, 0V to 0.6V amplitude logic 0
Impedance	75 ohms
Interface	Rear panel BNC connector
Phasing	Positive clock center of data. Internally strappable to negative clock in center of data.
DATA PATTERNS	
PRBS Unframed:	
DS1	$2^{20}-1$ PRBS with 14–zero constraint
DS1C	$2^{20}-1$ PRBS at the DS1C rate
DS2	$2^{20}-1$ PRBS at the DS2 rate
PRBS Framed:	
DS1	$2^{20}-1$, with 14–zero constraint (before framing) at 1.536-Mb/s rate with 8-kHz frame information inserted.
DS1C	Two PRBS multiplexed into a 3.152-Mb/s DS1C signal with DS1C frame and bit stuff control information.
DS2	Four PRBS multiplexed into a 6.312-Mb/s DS2 signal with DS2 frame and bit stuff control information.
All Ones	Framed or unframed
Fixed Short Pattern	Framed or unframed programmable repeating sequence. Both pattern content and pattern length (16–24 bits) programmable by rear panel DIP switches.
Thru Data	Internal connection of received data to transmitter output with error and/or jitter injection capability provided.
X-Bit	For DS1C or DS2 level signals. Normal logic "1."

FRAMING

Unframed	No framing bits
Framed:	
DS1	193 bits/frame
DS1C	1272 bits/master frame with 24 control bits
DS2	1176 bits/master frame with 24 control bits

ERROR INJECTION MODES

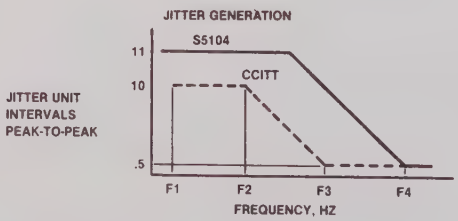
General	Error modes are valid for all patterns and rates.
Error Free	No errors generated
Internal Error Inject:	
Bit BPV	Inject rate 1×10^{-8} to 9×10^{-3} with mantissa and exponent units selectable. BPV's inserted without generating bit errors and without violating the B6ZS code in the DS2 mode or the B8ZS code in the DS1 mode.
Bit	Bit errors inserted in all bits (framing and information bits). Zero constraint not maintained.
Single Error Inject:	
Method	Front panel pushbutton
BPV	Single BPV error without bit errors and without violation of B6ZS or B8ZS codes.
Logic (Bit)	Single bit errors without BPV errors or without violation of 14–zero constraint. Valid in error-free mode. Errors in information (data) bits only. No single bit error in the THRU mode.
External Error Inject:	
Signal	Pulse = 1.0V peak-to-peak minimum/4.0V peak-to-peak maximum amplitude, 1 error/rising edge of input signal, 0.25 micro sec. minimum pulse width.
Interface	Rear panel BNC connector.
Impedance	600 ohms, AC-coupled.

MONITORS

General	0.040 in. (0.10 cm) diameter test point jacks with a ground jack provided. Minimum of 2.5 Vdc into 75 ohms driving 10 ft (3m) of cable.
Error Sync	Pulse synched to error insertion location.
M Sync Out	M frame sync in the DS1C or DS2 framed mode.
PR Sync Out	Pattern start sync. Indicates start of PRBS sequence.

JITTER

General	Timing jitter added to NRZ clock and data and to bipolar DS1, DS1C, or DS2 output (frequency and amplitude).
Internal Modulation:	
General	Jitter generation using internal sinewave source.
Modulation Limits	Meets or exceeds CCITT recommendations 0.171 (see Fig. 31).



	F1	F2			F3			F4		
		DS1	DS1C	DS2	DS1	DS1C	DS2	DS1	DS1C	DS2
CCITT	2	200	—	1600	4k	—	32k	40k	—	160k
S5104	10	500	1k	2k	11k	22k	44k	40k	80k	160k

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Fig. 31 – Jitter Generation

JITTER (Con't)

Amplitude Resolution	0.05 UI (Unit Intervals)
Amplitude Accuracy	±5% ±0.1 UI
Intrinsic Jitter	0.025 UI typical
Frequency Resolution	5% of the selected exponent
Frequency Accuracy	±5%
External Modulation:	
General	Jitter generation using an external modulation source. The peak-to-peak voltage is measured and displayed in Unit Intervals on the Transmitter display.
Interface	Rear panel BNC, 600 ohm impedance
Scaling	0.5V/UI peak-to-peak (2.75V peak maximum)
Modulation Limits	Meets or exceeds CCITT recommendations 0.171.
Amplitude Accuracy	±5% ±0.1 UI
Display Resolution	0.04 UI
Display Updated	Every two seconds. Measures amplitude down to 1 Hz.
Jitter Injection:	Jitter injection in the THRU mode from internal or external modulation source. Maximum jitter in the THRU mode is 10 UI.

9.2 RECEIVER SPECIFICATIONS

INPUT

Frequency	Clock recovered from input signal. Timing recovery using a phase lock loop with response tailored to communication test set requirements for DS1, DS1C, and DS2 signals.
Code	AMI for DS1 and DS1C. B6ZS for DS2. DS1 B8ZS Selectable.
Level:	
DS1	±3.0V plus up to 750 ft (228.8m) ABAM cable +6dB to −26dB
DS1C	±3.0V plus up to 655 ft (199.8m) ABAM cable +6dB to −26dB
DS2	DSX2 = ±2.1V plus up to 1000 ft (305m) ABAM cable +6dB to −43dB DS2H = ±2.1V, +6dB to −26dB
Interface	Two front panel connectors (WECo 310 plug-compatible) which are selectable by a front panel pushbutton or through remote control.
Impedance	110 ohms, balanced.

BINARY SIGNAL INPUTS

Data and Clock	Amplitude=2.5V to 5.0V, 0V baseline. Positive clock edge in center of data bit, internally strappable to negative clock edge. Rear panel BNC connectors accept 75-ohm impedance and bypass bipolar decoding and timing recovery.
Clock Frequency Range	1 MHz to 7 MHz

DATA PATTERNS

PRBS:	
Framed	$2^{20}-1$ sequence with 14-zero constraint. Demuxed to DS1 in DS1C/DS2 mode.
Unframed	$2^{20}-1$ sequence at data rate.
Programmed	Short patterns (16-24 bit) framed and unframed.

FRAMING

Unframed	No framing bits. Valid for all rates and patterns.
Framed	DS1, DS1C, DS2 frame synchronization. DS1C descrambling and DS1C/DS2 demultiplexing. Proprietary algorithm provides fast acquisition and high error tolerance.

CHANNEL SELECT

General	In framed PRBS mode, data is demultiplexed into channels 1 through 4 for DS2 and channels 1 and 2 for DS1C.

MONITORS

General	0.040 in. (0.10 cm) diameter test points with a minimum of 2.5 Vdc into 75 ohms capable of driving 10 ft (3m) of cable. Ground provided.
Bit Errors	Bit error output.
BPV Errors	Bipolar violation error output.
M Sync Out	M frame sync for DS1C and DS2 levels in the framed mode.
PR Sync Out	PRBS sync.

DISPLAY

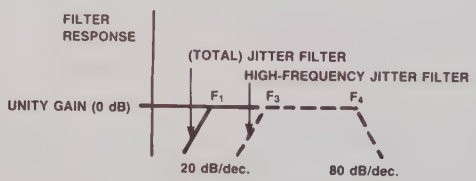
Alphanumeric	10-character vacuum-fluorescent display which displays all bit, BPV, frame, status, and time measurements.
Status	Present and history status of signal loss, frame loss, data sync loss, excess zeros, all ones, and X bit.

MEASUREMENTS

General	Simultaneously measures errors, status, and jitter depending on the Receiver input settings.
Errors:	
Total Errors	Total errors over elapsed time of test.
Average Error Rate	Average error rate over time of test.
Current Error	Current error rate over 10^7 bits. Not measured for frame errors.
Err-Secs	Synchronous errored seconds, internally strappable to asynchronous errored seconds.
Threshold Err-Secs	Synchronous threshold errored seconds, 10^{-5}, 10^{-4} and 10^{-3} error rates, errored seconds in which error rate exceeds the threshold. Not measured for frame errors.
Dribbling Total	Dribbling total errors, accumulation of all errors where the error rate is 10^{-6} in an errored second. Not measured for frame errors.
Status Event Seconds	Individual accumulation of number of synchronous or asynchronous errored seconds in which the following occurred: signal loss, frame loss, data sync loss, excess zeros, all ones and X bit.

JITTER

General	Simultaneously measures +and −peak jitter, peak-to-peak jitter, jitter threshold seconds, maximum jitter, and high-frequency jitter.
Jitter Measurement:	
Display Resolution	0.025 UI rounded up to the nearest 1/100 UI
Calculated Resolution	0.025 UI
Peak-To-Peak Accuracy	±5% ±0.1 UI
+and−Peak Accuracy	±5% ±0.1 UI
Filter Frequency Response	Consistent with T1X1 draft recommendations (see Fig. 32)



	F_1	F_3	F_4
DS1	10 Hz	8 kHz	68 kHz*
D1C	10 Hz	2 kHz	135 kHz*
DS2	10 Hz	3 kHz	270 kHz*

*Exceeds T1X1 value of 40 kHz for more accurate high-frequency jitter measurement.

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Fig. 32 – Jitter Tolerance

JITTER (Con't)

Demodulated Peak-To-Peak Jitter Output:	
Interface	Rear panel BNC, 75 ohms impedance, DC-coupled output
Accuracy	±5% ±0.1 UI
Scaling	0.8 volts UI peak-to-peak
Jitter Threshold Seconds	Seconds are counted during which either the peak-to-peak jitter amplitude or high-frequency jitter amplitude equals or exceeds a user-programmable threshold. Errored-second printouts will indicate either the current peak-to-peak jitter amplitude or the current high-frequency jitter amplitude depending on which is selected for jitter threshold seconds.

Jitter Receiver Bit Rate Tolerance

DS Rate	Bit Rate Tolerance
DS1	1.544 MHz±75 ppm
DS1C	3.152 MHz±35 ppm
DS2	6.312 MHz±35 ppm

TIMED MODES

Untimed	Continuous accumulation of all measurements and elapsed time.
Single	Accumulation of all measurements for duration of test. Test time programmable from 1 second to 1 second less than 100 days. If a printer is connected to the RS-232C or GPIB interface, all test results are automatically printed at the conclusion of a test.
Repeat	Accumulation of all measurements for programmable interval from 1 second to 1 second less than 100 days. At end of interval, test results are reset and the test is started again. Results of last completed test interval are stored for recall. If a printer is connected to the RS-232C or GPIB interface, all test results are automatically printed at the conclusion of a test.

9.3 GENERAL SPECIFICATIONS

GENERAL SPECIFICATIONS

Physical	Height—6.6 in. (16.7 cm) Width—13.6 in. (34.5 cm) Depth—17.1 in. (43.4 cm) Weight—16 lb (7.2 kg) Rubber feet on bottom Carrying handle on side Cover for front panel contains 6 ft (1.8m) AC power cord & fuse
Environmental	Temp—0° to 50°C (32° to 122°F)
Power	115 or 230 Vac±10% 40 to 66 Hz

OPTIONS

OP-05 Jitter Injection/Measurement
OP-06 Rackmount Kit, 8.75 in. (22.2 cm) height
OP-07 Model 5902 40-Column Compatible Thermal Printer (RS-232C)
OP-08 5910A Power Converter, −48 Vdc in/115 Vac out
OP-09 Hard-Shell Shipping Case
OP-10 Soft Carrying Case
OP-11 220 Vac Operation

SECTION 10
SERVICE AND MAINTENANCE

10.1 ASSISTANCE

For service assistance call the Tau-tron Customer Service Department, (617) 692-5100 or 1-800-TAU-TRON. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

10.2 REPAIR RETURNS

If you determined that your S5104 must be returned to the factory for repair, use the Repair Returns Card at the back of this manual and follow the directions to ensure prompt service.

10.3 ROUTINE SERVICE

The fan air filter on the S5104 rear panel must be vacuumed periodically. The dustier the working environment, the more frequently this task must be performed.

WARNING: Failure to keep the fan air filter clean may result in the S5104 overheating, causing damage to the unit.

Other than occasionally cleaning the exterior surface with a mild cleaner, no other periodic maintenance of the S5104 is required.

10.4 GENERAL TROUBLESHOOTING

WARNING: Do not attempt access to the inner PC boards without disconnecting the line cord from the power receptacle.

Printed Circuit Boards

PC boards may have loosened in the sockets or ribbon cables may be disconnected. If so, perform the following steps:

STEP	PROCEDURE
1	Remove top enclosure to gain access to the PC boards in the equipment.
2	Be sure all PC boards are properly seated in the connectors.
3	Be sure all interconnecting ribbon cables are properly secured to the PC boards.
4	Replace top enclosure removed in step 1.

DC Voltage

The Power Supply provides the +5V ±0.5V used throughout the system. To determine if the supply is operating properly, perform the following procedure.

STEP	PROCEDURE
1	Set the **POWER** switch to on; the **POWER** indicator lights.
2	If all the indicators on the front control panel illuminate when the AC power is first applied, the power supply is producing the required voltage. ***NOTE: After a few seconds, some of the indicators extinguish, putting the equipment in a ready, normal state for operation.***

Nicad Battery Cells

Your S5104 is equipped with three nicad rechargeable battery cells of 1.2 Vdc each, producing a **POWERLOSS** and **RECALL** backup. The batteries charge when the S5104 is powered ON and will fully charge overnight. Once fully charged, they hold the charge for more than one year. If the battery cells are discharged or disconnected, the power-up condition, from a power failure and recall, will be incorrect. These cells are located on the Front Panel Control PC boards and are of the GOULD 50 BL, 1.2V type. The cell performance can be checked as follows.

STEP	PROCEDURE
1	Connect a patch cable between **OUTPUT-DS1/1C/2** (left) jack and **INPUT-DS1/1C/2** (left) jack.
2	Set the equipment **POWER** switch to on; all the front-panel indicators light. ***NOTE: After a few seconds, some of the indicators extinguish, putting the unit in a ready, normal state for operation.***

STEP	PROCEDURE
3	Remove the unit power plug from the AC power source (do not turn the **POWER** switch to off on the S5104). ***NOTE: Setup state and measurements are not retained when the* POWER *is turned off from the front-panel switch. All front-panel indicators then extinguish.***
4	Replace the power plug removed from the AC power source; the front-panel indicators light and the **RECEIVER** display flashes **POWER LOSS**. The last configuration of data was stored in memory when the power was lost. ***NOTE: Even when the power is lost, the internal clock continues to keep time.***
5	Press any front-panel pushbutton; the **RECEIVER** display **POWER LOSS** extinguishes and **O TOT** is displayed.

10.5 FAILURE MESSAGES

If your S5104 does not operate correctly and displays **FAILURE XX**, refer to Table F. Call the Tau-tron Customer Service Department, (800) TAU-TRON (Outside MA) or (617) 692-5100.

TABLE F
S5104 FAILURE MESSAGES

NO.	FAILURE
01	Invalid memory access attempted.
02	Non-supported interrupt generated.
10	Unable to read/write to RAM properly.
11	ERROM checksum failure.
20	Unable to clear bit errored-second flag.
21	Unable to clear BPV errored-second flag.
22	Software error – Invalid run state.
23	Jitter installed but unable to read A/D.
30	Software throughout error.
31	Unable to generate requested jitter amplitude.
40	Invalid key process state.
41	Invalid key process state.
42	More than 1×10^{10} errors in 1×10^{7} bits.

FOR FUTURE UPDATES

If you want to receive updates or revised issues of this manual, please complete and mail the postage paid card below. *If you fail to do so, important updated information pertaining to this document will not be forwarded to you.*

If you would like a representative to call, require additional information on Tau-tron products, or would like to be placed on our mailing list, please complete and mail the *lower* postage paid card.

Instruction Manual Form Number: ☐☐☐☐☐–☐☐☐☐☐

☐ Yes, I would like to receive technical updates and revised issues of this document. I have filled in the manual form number above (Form No. is shown on title page).

to: Publications Manager

from:

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State & Zip _____ Phone _____

Please —

☐ Have representative call.

☐ Add me to your mailing list.

Send additional information on:

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☐ TDM Voice/Data Multiplexers
☐ Digital Transmission Test Sets
☐ Fiber Optic Transmission
☐ Data Loggers
☐ High Speed Components

My general application is _____

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Tau-tron Inc.
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Westford, MA. 01886

Repair Returns

To return a unit for repair:

1. Call the Customer Service Dept. **(617) 692-5100** or **1-800-TAU-TRON (outside MA),** for a **Repair Authorization Number.** This will reduce administrative delays and ensure prompt return of your unit.
2. Complete and **attach one of the Repair Tags** below to your unit.
3. **Pack the unit** in the original shipping carton and packaging materials, if available. Otherwise use a double-walled carton (test strength of 350 lb) and shock absorbing material such as bubble wrap to prevent the unit from moving in the carton during transit. Seal with heavy paper tape.
4. **Send to:**

   Tau-tron
   10 Lyberty Way
   Westford, MA 01886
   attn: Customer Service

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Form 0163-1181A

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

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